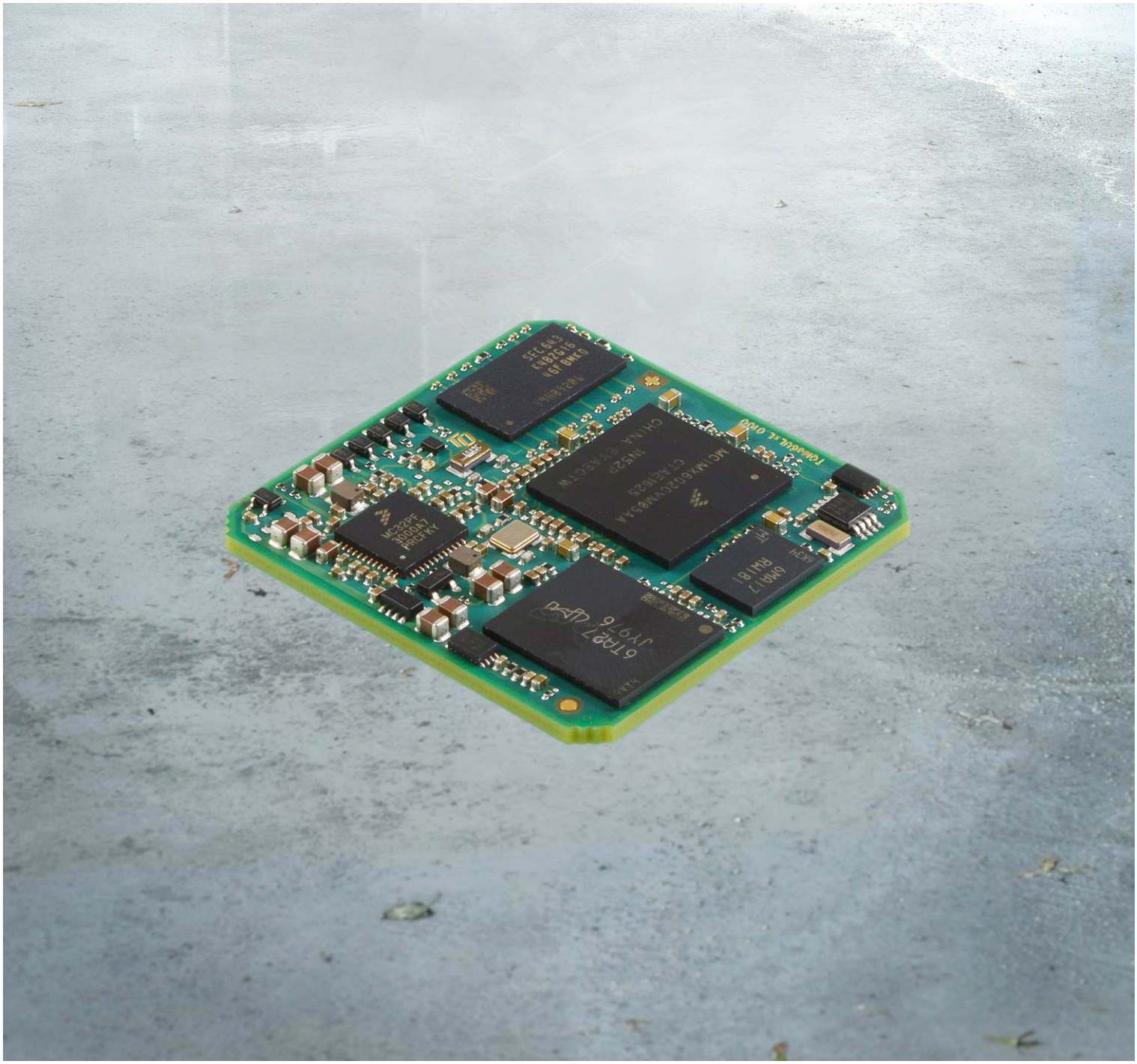
TQMa6ULxL
User's Manual

TQMa6ULxL UM 0100
17.05.2017



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	17.05.2017	Petz		First issue

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa6ULxL and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram MBa6ULx
- CPU Reference Manual IMX6ULxRM
- User's Manual MBa6ULx
- Documentation of boot loader U-Boot (http://www.denx.de/wiki/U-Boot/Documentation)
- Documentation of PTXdist (http://www.ptxdist.de)

2. BRIEF DESCRIPTION

This User's Manual describes the TQMa6ULxL and refers to some software settings. The TQMa6ULxL is the BGA-version of the TQMa6ULx. A certain derivative of the TQMa6ULxL does not necessarily provide all features described in this User's Manual. This User's Manual does also not replace the NXP CPU Reference Manual (6).

The TQMa6ULxL is a universal Minimodule based on the NXP ARM CPU MCIMX6G3CVM05 (i.MX6ULx).

The Cortex® A7 core of this CPU works typically with 528 MHz. [1]

2.1 Block diagram i.MX6ULx CPU

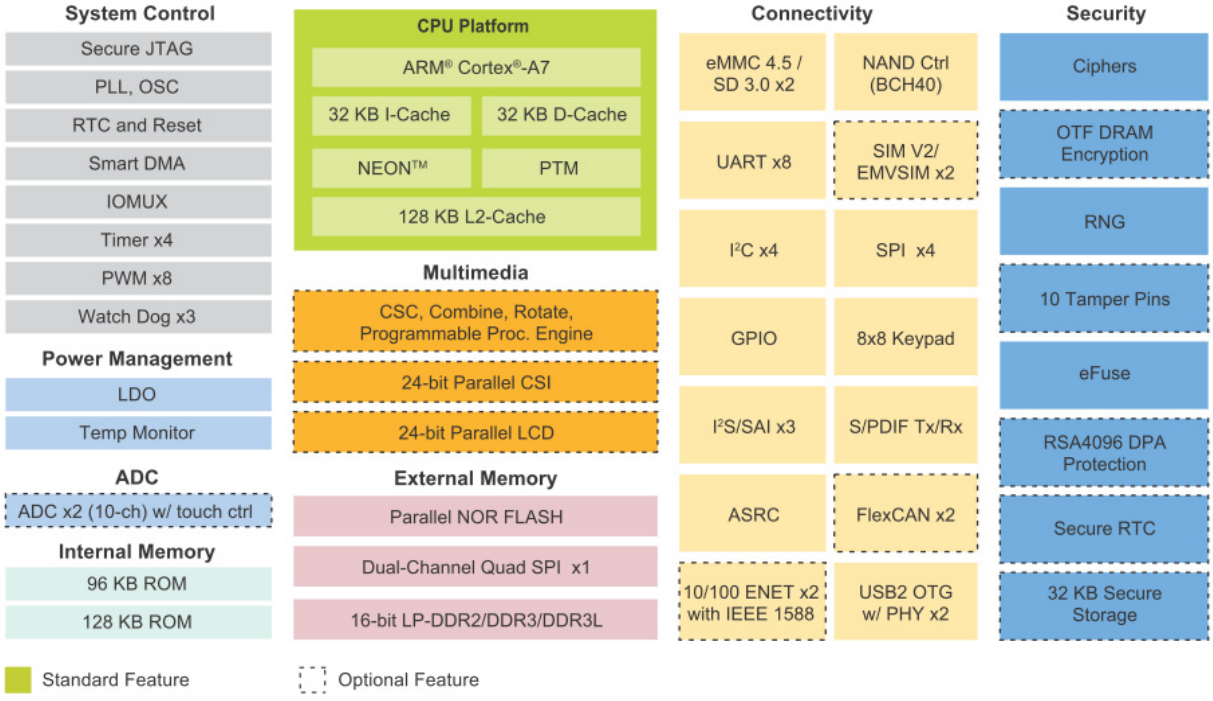

Illustration 1: Block diagram i.MX6ULx CPU
(Source: NXP)

The TQMa6ULxL extends the TQ-Systems GmbH product range and offers an outstanding computing performance.
A suitable CPU derivative (UL1, UL2, and UL3) can be selected for each requirement.
All essential CPU pins are routed to the TQMa6ULxL balls. There are therefore no restrictions for customers using the TQMa6ULxL with respect to an integrated customised design. All essential components like CPU, DDR3L SDRAM, eMMC, and power management are already integrated on the TQMa6ULxL.
The main features of the TQMa6ULxL are:

- NXP i.MX6ULx CPU
- Up to 1 Gbyte DDR3L SDRAM with 16 bit interface (standard: 256 Mbyte)
- Up to 32 Gbyte eMMC NAND flash (standard: 4 Gbyte)
- Up to 256 Mbyte QSPI NOR flash (standard: 32 Mbyte)
- 64 kbit EEPROM
- Manufacturer EEPROM (128 byte for protection mode, 128 byte for normal usage)
- Temperature sensor
- NXP Power Management Integrated Circuit PF3000
- All essential CPU pins are routed to the TQMa6ULxL balls
- Extended temperature range
- Single supply voltage 3.3 V

The combination “MBa6ULx” plus adapter “TQMa6ULxL_MB-Adap” serves as an evaluation board for the TQMa6ULxL.
The adapter comprises a 5 V to 3.3 V LDO to supply the TQMa6ULxL.

1: Up to 700 MHz with selected i.MX6ULx.

2.2 Key functions and characteristics

The following components are implemented on the TQMa6ULxL:

- i.MX6ULx CPU
- DDR3L SDRAM
- eMMC NAND flash
- QSPI NOR flash
- EEPROM
- Manufacturer EEPROM with temperature sensor
- RTC
- Supervisor with Reset structure
- Power supply by PMIC with Power Sequencing and 3.3 V direct via adapter
- 226 ball BGA

The following interfaces are provided at the TQMa6ULxL balls: [2]

- 2 × Ethernet 10/100 RMII
- 2 × I²C (1 × for the I²C devices on the TQMa6ULxL)
- 1 × JTAG
- 1 × Parallel LCD RGB 24-bit interface
- 2 × CAN
- 2 × I²C
- 1 × SPI
- 2 × USB 2.0 OTG
- 11 × GPIO
- 3 × UART
- 1 × SD 4-bit (SDIO / MMC / SD card)
- 10 × Tamper
- 1 × differential clock (CCM)
- 1 × QSPI (for second SPI NOR flash; SS1)
- 1 × WDOG1

By adapting the pin configuration, further i.MX6ULx interfaces are also available as an alternative to the factory configuration. These are amongst others:

- Camera Sensor-Interfaces 8-bit (CSI – CMOS Sensor Interface)
- Synchronous Audio Interface (SAI – e.g., I²S)
- PWM
- ADC
- NAND flash interface
- EIM bus (External Interface Module)
- Enhanced Periodic Interrupt Timer
- General Purpose Media Interface
- General Purpose Timer
- Keypad Port
- More audio interfaces
- One more I²C interface
- More SPI interfaces
- More UARTs

2: Number of interfaces depends on the i.MX6ULxL derivative.

3. ELECTRONICS

The information in this User's Manual is only valid in connection with the boot loader adapted for the TQMa6ULxL, which is preinstalled on every TQMa6ULxL (see also section 5) and the BSP provided by TQ-Systems GmbH.

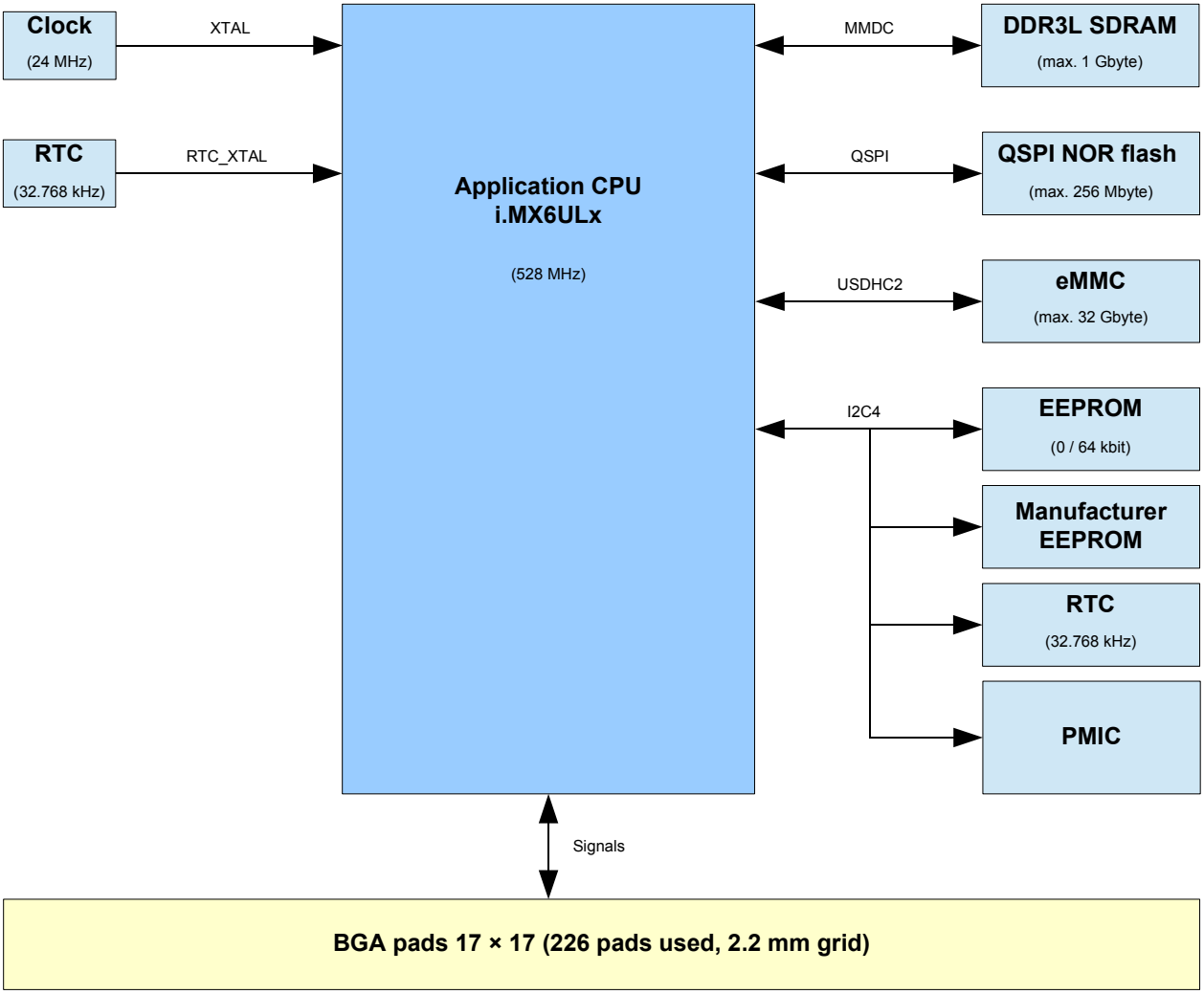

Illustration 2: Block diagram TQMa6ULxL (simplified)

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of. The pin assignment listed in Table 2 refers to the corresponding standard BSP provided by TQ-Systems GmbH in combination with the Starterkit MBa6ULx.

NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).

The electrical and pin characteristics are to be taken from the CPU Data Sheets (1), (2), (5), the CPU Reference Manual (6), and the PMIC Data Sheet (7).

3.1.2 BGA pad-out

Attention: Destruction or malfunction	
	Depending on the configuration, many CPU pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX6ULx Reference Manual (6), before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa6ULxL. The information given in the following sections is to be taken note of: RFU: Reserved pins without function. These pins may not be connected to support future versions of the TQMa6ULxL. NA: These pins may not be connected under any circumstances and have to be left open. (No BGA pad present.)

The TQMa6ULxL provides 226 pads. The following table shows the top view of the pad-out with i.MX6UL2 or i.MX6UL3 CPU. Please take note of the different i.MX6UL1 pad-out!

3.1.2.1 Pinout TQMa6ULxL

Table 2: Pinout TQMa6ULxL, **TOP VIEW through TQMa6ULxL**

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
17	NA	CCM_ CLK1_P	CCM_ CLK1_N	DGND	USB_ OTG1_DN	DGND	USB_ OTG1_DP	DGND	USB_ OTG2_DN	USB_ OTG2_DP	UART1_ TX_DATA	GPIO1_ IO18	GPIO1_ IO09	UART3_ TX_DATA	CAN1_ TX	MX6UL_ ONOFF	NA
16	VIN	VIN	DGND	USB_ OTG1_CHD#	DGND	USB_ OTG1_VBUS	DGND	USB_ OTG2_PWR	DGND	USB_ OTG2_VBUS	UART1_ RX_DATA	GPIO1_ IO19	DGND	UART3_ RX_DATA	CAN1_ RX	DGND	PMIC_ PWRON
15	VIN	VIN	VSNVS_ REF_OUT	DGND	VCCDDR_ OUT	USB_ OTG1_PWR	USB_ OTG1_OC	USB_ OTG2_ID / SD_VSEL	USB_ OTG2_OC	DGND	DRAM_ SDQS0_N	DRAM_ SDQS0_P	SNVS_ TAMPER4	DRAM_ SDCLK0_P	DRAM_ SDCLK0_N	DGND	RESET_ OUT#
14	VIN	VIN	LICELL	VCC2V5_ OUT	VCC3V3_ V33_OUT	USB_ OTG1_ID	DGND	SNVS_ TAMPER0	SNVS_ TAMPER1	SNVS_ TAMPER2	DRAM_ D5	DGND	SNVS_ TAMPER3	DGND	DRAM_ A0	RESET_ IN#	BOOT_ MODE1
13	DGND	DGND	DGND	DGND	NVCC_ ENET	NA	NA	NA	NA	NA	NA	NA	DGND	SNVS_ TAMPER5	SNVS_ TAMPER6	DGND	BOOT_ MODE0
12	DGND	DGND	DGND	DGND	NA	NA	NA	NA	NA	NA	NA	NA	NA	SNVS_ TAMPER7	SNVS_ TAMPER8	CAN2_ RX	CAN2_ TX
11	SPI2_ SCLK	SPI2_ SSO#	SPI2_ MOSI	SPI2_ MISO	NA	NA	JTAG_ TMS	DGND	JTAG_ TRST#	DGND	VDDSOC_ CAP	NA	NA	SNVS_ TAMPER9	DGND	I2C4_ SDA	I2C4_ SCL
10	DGND	DGND	VCC3V3_ REF_OUT	VCCCORE_ OUT	NA	NA	JTAG_ TDI	NA	NA	NA	DGND	NA	NA	SD1_ DATA0	SD1_ CMD	DGND	SD1_ CLK
9	VCC3V3_ IN	VCC3V3_ IN	WDOG1#	VCC1V8_ OUT	NA	NA	JTAG_ TDO	NA	NA	NA	DGND	NA	NA	DGND	SD1_ DATA3	SD1_ DATA2	SD1_ DATA1
8	ENET1_ TDATA0	ENET1_ TDATA1	DGND	DGND	NA	NA	DGND	NA	NA	NA	VDDSOC_ CAP	NA	NA	UART6_ RX_DATA	UART6_ TX_DATA	DGND	I2C2_ SCL
7	ENET1_ TX_CLK	DGND	ENET1_ TX_EN	DGND	NA	NA	JTAG_ MOD	DGND	JTAG_ TCK	DGND	VDDARM_ CAP	NA	NA	DGND	GPIO4_ IO22	GPIO4_ IO21	I2C2_ SDA
6	ENET1_ RDATA0	ENET1_ RDATA1	DGND	ENET_ MGMT_MDC	DGND	NA	NA	NA	NA	NA	NA	NA	NA	GPIO4_ IO25	GPIO4_ IO24	DGND	GPIO4_ IO23
5	ENET1_ RX_EN	DGND	ENET1_ RX_ER	ENET_ MGMT_ MDIO	eMMC_ SCK	DGND	NA	NA	NA	NA	NA	NA	NVCC_ CSI	DGND	GPIO4_ IO28	GPIO4_ IO27	GPIO4_ IO26
4	ENET2_ TDATA0	ENET2_ TDATA1	DGND	DGND	eMMC_ CMD	eMMC_ RST#	QSPI_ A_SS1#	QSPI_ A_SCK	LCD_ DATA23	LCD_ DATA19	LCD_ DATA16	LCD_ DATA12	LCD_ DATA09	LCD_ DATA05	DGND	LCD_ RESET	LCD_ VSYNC
3	ENET2_ TX_CLK	DGND	ENET2_ TX_EN	eMMC_ DATA6	DGND	eMMC_ DATA5	QSPI_ A_SS0#	DGND	LCD_ DATA22	LCD_ DATA18	LCD_ DATA15	LCD_ DATA11	LCD_ DATA08	LCD_ DATA04	LCD_ DATA02	DGND	LCD_ HSYNC
2	ENET2_ RDATA0	ENET2_ RDATA1	DGND	eMMC_ DATA7 / QSPI_ A_SS1#	eMMC_ DATA4	eMMC_ DATA3	QSPI_ A_DATA1	QSPI_ A_DATA0	LCD_ DATA21	DGND	LCD_ DATA14	DGND	LCD_ DATA7	DGND	LCD_ DATA01	DGND	LCD_ ENABLE
1	NA	ENET2_ RX_EN	ENET2_ RX_ER	eMMC_ DATA2	eMMC_ DATA1	eMMC_ DATA0	QSPI_ A_DATA3	QSPI_ A_DATA2	LCD_ DATA20	LCD_ DATA17	LCD_ DATA13	LCD_ DATA10	LCD_ DATA06	LCD_ DATA03	LCD_ DATA00	LCD_ CLK	NA
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U

The secondary functions of CSI and NAND flash interfaces are pattern coded as follows:

Illustration 3: Secondary function of some TQMa6ULxL BGA pads

3.1.2.2 TQMa6ULxL signals

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX6ULx CPU Data Sheets (1), (6) and the PMIC Reference Manual (7).

Table 3: TQMa6ULxL, signals

CPU ball	I/O	Level	Group	Signal	TQMa6ULxL ball
T10	I	3.0 V [3]	Boot	BOOT_MODE0	U13
U10	I	3.0 V [3]	Boot	BOOT_MODE1	U14
G14	I	3.3 V	CAN	CAN1_RX	R16
H15	O	3.3 V	CAN	CAN1_TX	R17
H14	I	3.3 V	CAN	CAN2_RX	T12
J15	O	3.3 V	CAN	CAN2_TX	U12
P16	O	2.5 V	CCM	CCM_CLK1_N	C17
P17	O	2.5 V	CCM	CCM_CLK1_P	B17
R8	I	3.3 V	Config	MX6UL_ONOFF	T17
T9	I	3.3 V	Config	PMIC_PWRON	U16
P8	I	3.3 V	Config	RESET_IN#	T14
–	O	3.3 V	Config	RESET_OUT#	U15
N17	O	3.3 V	Config	WDOG1#	C9
–	O	0.675 V	DRAM	DRAM_A0	R14
–	O	0.675 V	DRAM	DRAM_D5	L14
–	O		DRAM	DRAM_SDCLK0_N	R15
–	O		DRAM	DRAM_SDCLK0_P	P15
–	O	0.675 V	DRAM	DRAM_SDQS0_N	L15
–	O	0.675 V	DRAM	DRAM_SDQS0_P	M15
C8	I/O	3.3 V	EMMC	EMMC_CMD	E4
D7	I/O	3.3 V	EMMC	EMMC_DATA0	F1
B7	I/O	3.3 V	EMMC	EMMC_DATA1	E1
A7	I/O	3.3 V	EMMC	EMMC_DATA2	D1
D6	I/O	3.3 V	EMMC	EMMC_DATA3	F2
C6	I/O	3.3 V	EMMC	EMMC_DATA4	E2
B6	I/O	3.3 V	EMMC	EMMC_DATA5	F3
A6	I/O	3.3 V	EMMC	EMMC_DATA6	D3
B4	O	3.3 V	EMMC	EMMC_RST#	F4
D8	O	3.3 V	EMMC	EMMC_SCK	E5
L16	O	2.5 V / 3.3 V [4]	ENET	ENET_MGMT_MDC	D6
K17	I/O	2.5 V / 3.3 V [4]	ENET	ENET_MGMT_MDIO	D5
F16	I	2.5 V / 3.3 V [4]	ENET	ENET1_RDATA0	A6
E17	I	2.5 V / 3.3 V [4]	ENET	ENET1_RDATA1	B6
E16	I	2.5 V / 3.3 V [4]	ENET	ENET1_RX_EN	A5
D15	I	2.5 V / 3.3 V [4]	ENET	ENET1_RX_ER	C5
E15	O	2.5 V / 3.3 V [4]	ENET	ENET1_TDATA0	A8
E14	O	2.5 V / 3.3 V [4]	ENET	ENET1_TDATA1	B8
F14	O	2.5 V / 3.3 V [4]	ENET	ENET1_TX_CLK	A7
F15	O	2.5 V / 3.3 V [4]	ENET	ENET1_TX_EN	C7
C17	I	2.5 V / 3.3 V [4]	ENET	ENET2_RDATA0	A2
C16	I	2.5 V / 3.3 V [4]	ENET	ENET2_RDATA1	B2
B17	I	2.5 V / 3.3 V [4]	ENET	ENET2_RX_EN	B1
D16	I	2.5 V / 3.3 V [4]	ENET	ENET2_RX_ER	C1
A15	O	2.5 V / 3.3 V [4]	ENET	ENET2_TDATA0	A4
A16	O	2.5 V / 3.3 V [4]	ENET	ENET2_TDATA1	B4
D17	O	2.5 V / 3.3 V [4]	ENET	ENET2_TX_CLK	A3
B15	O	2.5 V / 3.3 V [4]	ENET	ENET2_TX_EN	C3

3: Use VSNVS_REF_OUT as reference voltage for BOOT-CFG resistors.
4: 2.5 V if NVCC_ENET is connected to VCC2V5_OUT. 3.3 V if NVCC_ENET is connected to VCC3V3_REF_OUT.

Table 3: TQMa6ULxL, signals (continued)

CPU ball	I/O	Level	Group	Signal	TQMa6ULxL ball
M15	I/O	3.3 V	GPIO	GPIO1_IO09	N17
K15	I/O	3.3 V	GPIO	GPIO1_IO18	M17
J14	I/O	3.3 V	GPIO	GPIO1_IO19	M16
E4	I/O	3.3 V [5]	GPIO	GPIO4_IO21	T7
E3	I/O	3.3 V [5]	GPIO	GPIO4_IO22	R7
E2	I/O	3.3 V [5]	GPIO	GPIO4_IO23	U6
E1	I/O	3.3 V [5]	GPIO	GPIO4_IO24	R6
D4	I/O	3.3 V [5]	GPIO	GPIO4_IO25	P6
D3	I/O	3.3 V [5]	GPIO	GPIO4_IO26	U5
D2	I/O	3.3 V [5]	GPIO	GPIO4_IO274	T5
D1	I/O	3.3 V [5]	GPIO	GPIO4_IO28	R5
F3	I/O	3.3 V	I2C	I2C2_SCL	U8
F2	I/O	3.3 V	I2C	I2C2_SDA	U7
J17	I/O	3.3 V	I2C	I2C4_SCL	U11
J16	I/O	3.3 V	I2C	I2C4_SDA	T11
P15	I	3.3 V	JTAG	JTAG_MOD	G7
M14	I	3.3 V	JTAG	JTAG_TCK	J7
N16	I	3.3 V	JTAG	JTAG_TDI	G10
N15	O	3.3 V	JTAG	JTAG_TDO	G9
P14	I	3.3 V	JTAG	JTAG_TMS	G11
N14	I	3.3 V	JTAG	JTAG_TRST#	J11
A8	O	3.3 V	LCD	LCD_CLK	T1
B9	I/O	3.3 V [6]	LCD	LCD_DATA00	R1
A9	I/O	3.3 V [6]	LCD	LCD_DATA01	R2
E10	I/O	3.3 V [6]	LCD	LCD_DATA02	R3
D10	I/O	3.3 V [6]	LCD	LCD_DATA03	P1
C10	I/O	3.3 V [6]	LCD	LCD_DATA04	P3
B10	I/O	3.3 V [6]	LCD	LCD_DATA05	P4
A10	I/O	3.3 V [6]	LCD	LCD_DATA06	N1
D11	I/O	3.3 V [6]	LCD	LCD_DATA07	N2
B11	I/O	3.3 V [6]	LCD	LCD_DATA08	N3
A11	I/O	3.3 V [6]	LCD	LCD_DATA09	N4
E12	I/O	3.3 V [6]	LCD	LCD_DATA10	M1
D12	I/O	3.3 V [6]	LCD	LCD_DATA11	M3
C12	I/O	3.3 V [6]	LCD	LCD_DATA12	M4
B12	I/O	3.3 V [6]	LCD	LCD_DATA13	L1
A12	I/O	3.3 V [6]	LCD	LCD_DATA14	L2
D13	I/O	3.3 V [6]	LCD	LCD_DATA15	L3
C13	I/O	3.3 V [6]	LCD	LCD_DATA16	L4
B13	I/O	3.3 V [6]	LCD	LCD_DATA17	K1
A13	I/O	3.3 V [6]	LCD	LCD_DATA18	K3
D14	I/O	3.3 V [6]	LCD	LCD_DATA19	K4
C14	I/O	3.3 V [6]	LCD	LCD_DATA20	J1
B14	I/O	3.3 V [6]	LCD	LCD_DATA21	J2
A14	I/O	3.3 V [6]	LCD	LCD_DATA22	J3
B16	I/O	3.3 V [6]	LCD	LCD_DATA23	J4
B8	O	3.3 V	LCD	LCD_ENABLE	U2
D9	O	3.3 V	LCD	LCD_HSYNC	U3
E9	O	3.3 V	LCD	LCD_RESET	T4
C9	I/O	3.3 V	LCD	LCD_VSYNC	U4
A5	O	3.3 V	QSPI	EMMC_DATA7/QSPI_A_SS1#	D2
A3	I/O	3.3 V	QSPI	QSPI_A_DATA0	H2
C5	I/O	3.3 V	QSPI	QSPI_A_DATA1	G2
B5	I/O	3.3 V	QSPI	QSPI_A_DATA2	H1
A4	I/O	3.3 V	QSPI	QSPI_A_DATA3	G1
D5	O	3.3 V	QSPI	QSPI_A_SCK	H4
E6	O	3.3 V	QSPI	QSPI_A_SS0#	G3
A5	O	3.3 V	QSPI	QSPI_A_SS1#	G4

5: 1.8 V if NVCC_CSI is connected to VCC1V8_OUT. 3.3 V if NVCC_CSI is connected to VCC3V3_V33_OUT.
6: Use VCC3V3_REF_OUT as reference voltage for BOOT-CFG resistors.

Table 3: TQMa6ULxL, signals (continued)

CPU ball	I/O	Level	Group	Signal	TQMa6ULxL ball
C1	O	3.3 V	SD	SD1_CLK	U10
C2	I/O	3.3 V	SD	SD1_CMD	R10
B3	I/O	3.3 V	SD	SD1_DATA0	P10
B2	I/O	3.3 V	SD	SD1_DATA1	U9
B1	I/O	3.3 V	SD	SD1_DATA2	T9
A2	I/O	3.3 V	SD	SD1_DATA3	R9
R10	I	3.3 V	SNVS	SNVS_TAMPER0	H14
R9	I	3.3 V	SNVS	SNVS_TAMPER1	J14
P11	I	3.3 V	SNVS	SNVS_TAMPER2	K14
P10	I	3.3 V	SNVS	SNVS_TAMPER3	N14
P9	I	3.3 V	SNVS	SNVS_TAMPER4	N15
N8	I	3.3 V	SNVS	SNVS_TAMPER5	P13
N11	I	3.3 V	SNVS	SNVS_TAMPER6	R13
N10	I	3.3 V	SNVS	SNVS_TAMPER7	P12
N9	I	3.3 V	SNVS	SNVS_TAMPER8	R12
R6	I	3.3 V	SNVS	SNVS_TAMPER9	P11
G13	I	3.3 V	SPI	SPI2_MISO	D11
F17	O	3.3 V	SPI	SPI2_MOSI	C11
G17	O	3.3 V	SPI	SPI2_SCLK	A11
G16	O	3.3 V	SPI	SPI2_SS0#	B11
K16	I	3.3 V	UART	UART1_RX_DATA	L16
K14	O	3.3 V	UART	UART1_TX_DATA	L17
H16	I	3.3 V	UART	UART3_RX_DATA	P16
H17	O	3.3 V	UART	UART3_TX_DATA	P17
E5	I	3.3 V	UART	UART6_RX_DATA	P8
F5	O	3.3 V	UART	UART6_TX_DATA	R8
U16	O	Open-Drain	USB	USB_OTG1_CHD#	D16
T15	I/O	3 V	USB	USB_OTG1_DN	E17
U15	I/O	3 V	USB	USB_OTG1_DP	G17
K13	I	3.3 V	USB	USB_OTG1_ID	F14
L15	I	3.3 V	USB	USB_OTG1_OC	G15
M16	O	3.3 V	USB	USB_OTG1_PWR	F15
T13	I/O	3 V	USB	USB_OTG2_DN	J17
U13	I/O	3 V	USB	USB_OTG2_DP	K17
M17	I	3.3 V	USB	USB_OTG2_ID/SD_VSEL	H15
L17	I	3.3 V	USB	USB_OTG2_OC	J15
L14	O	3.3 V	USB	USB_OTG2_PWR	H16
–	P	3.3 V	Power	VIN	A14, A15, A16, B14, B15, B16
–	P	3.3 V	Power	LICELL [7]	C14
F4	P	1.8 V / 3.3 V [8]	Power	NVCC_CSI	N5
F13	P	2.5 V / 3.3 V [9]	Power	NVCC_ENET	E13
T12	P	5 V	Power	USB_OTG1_VBUS	F16
U12	P	5 V	Power	USB_OTG2_VBUS	K16
–	P	1.8 V	Power	VCC1V8_OUT	D9
–	P	2.5 V	Power	VCC2V5_OUT	D14
–	P	3.3 V	Power	VCC3V3_IN	A9, B9
–	P	3.3 V	Power	VCC3V3_REF_OUT	C10
–	P	3.3 V	Power	VCC3V3_V33_OUT	E14
–	P	1.4 V	Power	VCCCORE_OUT	D10
–	P	0.675 V	Power	VCCDDR_OUT	E15
–	P	3.0 V	Power	VSNVS_REF_OUT	C15
–	P	1.2 V	VDDARM_CAP	VDDARM_CAP	L7
–	P	1.2 V	VDDSOC_CAP	VDDSOC_CAP	L8, L11
–	P	0 V	Ground	DGND	A10, A12, A13, B10, B12, B13, B3, B5, B7, C12, C13, C16, C2, C4, C6, C8, D12, D13, D15, D17, D4, D7, D8, E16, E3, E6, F17, F5, G14, G16, G8, H11, H17, H3, H7, J16, K11, K15, K2, K7, L10, L9, M14, M2, N13, N16, P14, P2, P5, P7, P9, R11, R4, T10, T13, T15, T16, T2, T3, T6, T8

7: LICELL can be left open if RTC-Backup or another function of the SNVS domain is not used (see NXP documentation).
8: 1.8 V if NVCC_CSI is connected to VCC1V8_OUT. 3.3 V if NVCC_CSI is connected to VCC3V3_V33_OUT.
9: 2.5 V if NVCC_ENET is connected to VCC2V5_OUT. 3.3 V if NVCC_ENET is connected to VCC3V3_REF_OUT.

3.2 System components

3.2.1 i.MX6ULx CPU

3.2.1.1 CPU derivatives

Depending on the TQMa6ULxL derivative, one of the following CPU derivatives is assembled.

Table 4: CPU derivatives

Description	CPU clock	Temperature range	Supported by TQ-BSP
MCIMX6G1CVM05AA [10]	528 MHz	–40 °C to +105 °C	Yes
MCIMX6G2CVM05AA	528 MHz	–40 °C to +105 °C	Yes
MCIMX6G3CVM05AA	528 MHz	–40 °C to +105 °C	Yes

3.2.1.2 CPU errata

Attention: Malfunction	
	Please take note of the current i.MX6ULx CPU errata (2).

3.2.1.3 Boot modes

The i.MX6ULx contains a ROM with integrated boot loader.
After power-up, the boot code initializes the hardware and then loads the program image from the selected boot device.
The eMMC or the QSPI NOR flash integrated on the TQMa6ULxL can for example be selected as the standard boot device.
Additional boot interfaces are available as an alternative to booting from the integrated eMMC or the QSPI NOR flash, see 3.2.1.5.
More information about boot interfaces and its configuration is to be taken from the CPU Data Sheet (1) and the CPU Reference Manual (6).
The boot device and its configuration, as well as different CPU settings have to be set via different boot mode registers.
Therefore, the i.MX6ULx provides two possibilities:

- Burning internal eFuses
- Reading dedicated GPIO pins

The exact behaviour during booting depends on the value of register BT_FUSE_SEL (default = 0).
The following table shows the behaviour of bit BT_FUSE_SEL in dependence of the boot mode selected.

Table 5: Boot modes and BT_FUSE_SEL

BOOT_MODE[1:0]	Boot type	Setting BT_FUSE_SEL	Recommended for
00 (default)	Boot From Fuses	0 = Boot using Serial Loader (Default) 1 = Boot mode configuration is taken from fuses.	Series production
01	Serial Downloader	n/a	Development / production
10	Internal Boot	0 = Boot mode configuration is taken from GPIOs. (Default) 1 = Boot mode configuration is taken from fuses.	Development
11	Reserved	n/a	n/a

10: Please take note of the different i.MX6UL1 pad-out!

3.2.1.4 Boot configuration

Some general settings are done with some eFuses independent from the boot device.

Table 6: General boot settings

Signal / eFuse	Pin name	CPU ball	TQMa6ULxL ball	Setting	Default	TQMa6ULxL [11]
BOOT_CFG1[7:0]	LCD_DATA[7:0]	D11,A10,B10, C10,D10,E10, A9,B9	N2,N1,P4, P3,P1,R3, R2,R1	**Boot configuration 1:** Specific to selected boot mode	–	0001 0000
BOOT_CFG2[7:3] BOOT_CFG2[1:0]	LCD_DATA[15:11] LCD_DATA[9:8]	D13,A12,B12, C12,D12, A11,B11	L3,L2,L1, M4,M3 N4,N3	**Boot configuration 2:** Specific to selected boot mode	–	–
BOOT_CFG2[2]	LCD_DATA10	E12	M1	**Boot frequencies (ARM / DDR):** 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	–
BOOT_CFG3[7:0]	–	–	–	**Reserved**	–	–
BOOT_CFG4[6:0]	LCD_DATA[22:16]	A14,B14,C14, D14,A13,B13, C13	J3,J2,J1, K4,K3,K1, L4	**Boot configuration 4:** Specific to selected boot mode	–	–
BOOT_CFG4[7]	LCD_DATA23	B16	J4	**Debug loop:** 0 = Loop disabled 1 = Loop enabled	0	–

Note: Boot configuration	
	No default boot device is preconfigured on the TQMa6ULxL at delivery.

3.2.1.5 Boot interfaces

The next sections describe the configuration of the following boot devices:

- eMMC
- QSPI NOR flash
- SD card

11: Recommended settings.

3.2.1.6 Boot device eMMC

Table 7: Boot configuration eMMC at USDHC2

Signal / eFuse	Pin name	CPU ball	TQMa6ULxL ball	Setting	Default	TQMa6ULxL [12]
BOOT_CFG1[7]	LCD_DATA07	D11	N2	**Boot Device Selection:** 01 = Boot from USDHC Interface	0	0
BOOT_CFG1[6]	LCD_DATA06	A10	N1		0	1
BOOT_CFG1[5]	LCD_DATA05	B10	P4	**SD/MMC Selection:** 0 = SD/eSD/SDXC 1 = MMC/eMMC	0	1
BOOT_CFG1[4]	LCD_DATA04	C10	P3	**Fast Boot:** 0 = Regular 1 = Fast boot	0	0
BOOT_CFG1[3]	LCD_DATA03	D10	P1	**MMC Speed:** 0x = Normal Speed Mode 1x = High Speed Mode	0	0
BOOT_CFG1[2]	LCD_DATA02	E10	R3		0	0
BOOT_CFG1[1]	LCD_DATA01	A9	R2	**eMMC Reset Enable:** 0 = No action 1 = eMMC reset enabled (SD_RST pad)	0	0
BOOT_CFG1[0]	LCD_DATA00	B9	R1	**SD Loopback Clock Source Selection:** 0 = Through SD pad 1 = Direct	0	0
BOOT_CFG2[7]	LCD_DATA15	D13	L3	**eMMC Bus Width:** 000 = 1-bit 001 = 4-bit 010 = 8-bit 101 = 4-bit DDR (MMC 4.4) 110 = 8-bit DDR (MMC 4.4)	0	0
BOOT_CFG2[6]	LCD_DATA14	A12	L2		0	1
BOOT_CFG2[5]	LCD_DATA13	B12	L1		0	0
BOOT_CFG2[4]	LCD_DATA12	C12	M4	**Port Select:** 00 = USDHC1 01 = USDHC2	0	0
BOOT_CFG2[3]	LCD_DATA11	D12	M3		0	1
BOOT_CFG2[2]	LCD_DATA10	E12	M1	**Boot Frequencies (ARM / DDR):** 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	0
BOOT_CFG2[1]	LCD_DATA09	A11	N4	**USDHC Voltage Selection:** 0 = 3.3 V 1 = 1.8 V	0	0

In addition to the mode listed above the following eMMC modes are supported at port USDHC2.

Table 8: USDHC2 modes eMMC

eMMC mode	1 bit	4 bit	8 bit	8 bit DDR
Normal speed	Yes	Yes	Yes	Yes
High-Speed (HS)	n/a	n/a	n/a	n/a

- High-Speed mode (HS) is not supported.

12: Recommended settings.

3.2.1.7 Boot device QSPI NOR flash

Table 9: Boot configuration QSPI NOR flash at QSPI1

Signal / eFuse	Pin name	CPU ball	TQMa6ULxL ball	Setting	Default	TQMa6ULxL [13]
BOOT_CFG1[7]	LCD_DATA07	D11	N2	**Boot Device Selection:** 0001 = Boot from QuadSPI	0	0
BOOT_CFG1[6]	LCD_DATA06	A10	N1		0	0
BOOT_CFG1[5]	LCD_DATA05	B10	P4		0	0
BOOT_CFG1[4]	LCD_DATA04	C10	P3		0	1
BOOT_CFG1[3]	LCD_DATA03	D10	P1	**QuadSPI Interface Selection:** 0 = QSPI1 1 = Reserved	0	0
BOOT_CFG1[2]	LCD_DATA02	E10	R3	**DDRSMP:** 000 = Default	0	0
BOOT_CFG1[1]	LCD_DATA01	A9	R2		0	0
BOOT_CFG1[0]	LCD_DATA00	B9	R1		0	0

13: Recommended settings.

3.2.1.8 Boot device SD card

Table 10: Boot configuration SD card at USDHC1

Signal / eFuse	Pin name	CPU ball	TQMa6ULxL ball	Setting	Default	TQMa6ULxL [14]
BOOT_CFG1[7]	LCD_DATA07	D11	N2	**Boot Device Selection:** 01 = Boot from USDHC Interface	0	0
BOOT_CFG1[6]	LCD_DATA06	A10	N1		0	1
BOOT_CFG1[5]	LCD_DATA05	B10	P4	**SD/MMC Selection:** 0 = SD/eSD/SDXC 1 = MMC/eMMC	0	0
BOOT_CFG1[4]	LCD_DATA04	C10	P3	**Fast Boot:** 0 = Regular 1 = Fast boot	0	0
BOOT_CFG1[3]	LCD_DATA03	D10	P1	**SD Speed:** 00 = Normal/SDR12 01 = High/SDR25 10 = SDR50 11 = SDR104	0	0
BOOT_CFG1[2]	LCD_DATA02	E10	R3		0	1
BOOT_CFG1[1]	LCD_DATA01	A9	R2	**SD Power Cycle Enable:** 0 = No power cycle 1 = Enable via USDHC_RST pad	0	0
BOOT_CFG1[0]	LCD_DATA00	B9	R1	**SD Loopback Clock Source Sel:** 0 = through SD pad 1 = direct	0	0
BOOT_CFG2[7]	LCD_DATA15	D13	L3	**SD Calibration Step:** 00 = 0 delay cells 01 = 1 delay cells 10 = 2 delay cells 11 = 3 delay cells	0	0
BOOT_CFG2[6]	LCD_DATA14	A12	L2		0	0
BOOT_CFG2[5]	LCD_DATA13	B12	L1	**Bus Width:** 0 = 1-bit 1 = 4-bit	0	1
BOOT_CFG2[4]	LCD_DATA12	C12	M4	**Port Select:** 00 = USDHC1 01 = USDHC2	0	0
BOOT_CFG2[3]	LCD_DATA11	D12	M3		0	0
BOOT_CFG2[2]	LCD_DATA10	E12	M1	**Boot Frequencies (ARM / DDR):** 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	0
BOOT_CFG2[1]	LCD_DATA09	A11	N4	**USDHC Voltage Selection:** 0 = 3.3 V 1 = 1.8 V	0	0

In addition to the mode listed above the following SD card modes are supported at port USDHC1.

Table 11: USDHC1 SD card modes

SD mode	Fast boot	1 bit	4 bit
Normal speed	Yes	Yes	Yes
High speed	Yes	Yes	Yes
SDR50	No	No	No
SDR104	No	No	No

14: Recommended settings.

3.2.2 Memory

The TQMa6ULxL standard variant contains the following memories:

- 256 Mbyte DDR3L SDRAM with 16 bit interface
- 4 Gbyte eMMC NAND flash
- 32 Mbyte QSPI NOR flash
- 64 kbit EEPROM
- 256 bytes Manufacturer EEPROM (128 byte for protection mode, 128 byte for normal usage)

3.2.2.1 DDR3L SDRAM

One DDR3L SDRAM chip is assembled on the TQMa6ULxL. The chip is connected to the CPU with a bus width of 16 bit. The following block diagram shows how the DDR3L SDRAM is connected to the CPU.

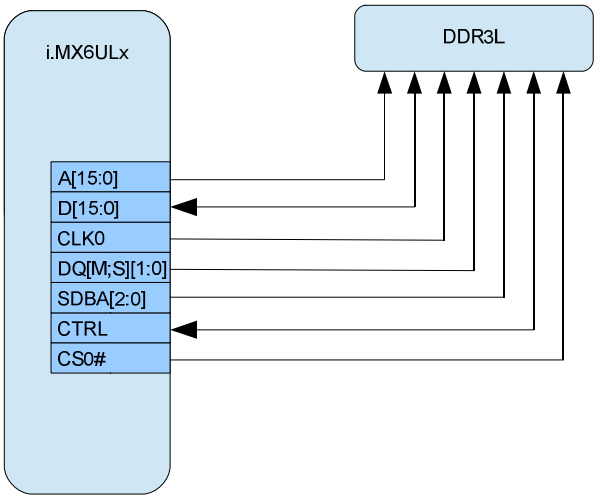

Illustration 4: Block diagram DDR3L SDRAM interface

The memory interface characteristics are shown in the following table.

Table 12: i.MX6ULx SDRAM interface

CPU derivative	Bus width	Frequency	No. of SDRAM chips	Supported by TQ-BSP
i.MX6ULx	×16	400 MHz	1	Yes

The assembly options of DDR3L SDRAM on the TQMa6ULxL are listed in the following table.

Table 13: DDR3L SDRAM

Manufacturer	Part number	Type	Temperature range
Micron	MT41K128M16JT-125 IT:K	DDR3L-1600 128M16	–40 °C to +95 °C
Samsung	K4B2G1646F-BMK0	DDR3L-1600 128M16	–40 °C to +95 °C

3.2.2.2 eMMC NAND flash

An eMMC NAND flash is provided for the boot loader and the application software.
The following block diagram shows how the eMMC flash is connected to the CPU.

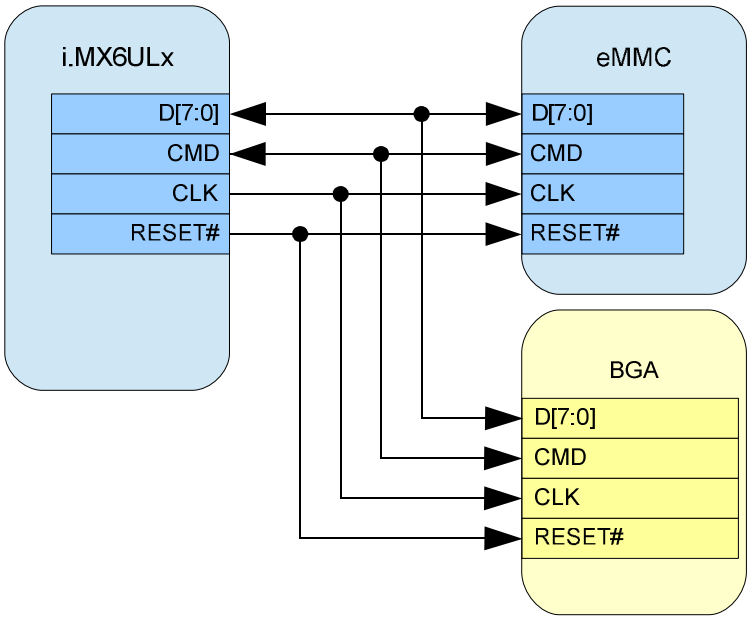

Illustration 5: Block diagram eMMC interface

It depends on the BSP implementation, whether the Hardware Reset-Function is supported.

The following table shows the eMMC devices, which can be assembled on the TQMa6ULxL.

Table 14: eMMC NAND flash

Manufacturer	Part number	Type	Temperature range
Micron	MTFC4GACAJCN-1M	4 Gbyte / eMMC 5.0 / MLC	–25 °C to +85 °C
Micron	MTFC4GACAJCN-4M	4 Gbyte / eMMC 5.0 / MLC	–40 °C to +85 °C

Attention: eMMC interface	
	The eMMC interface is not available when the eMMC is assembled on the TQMa6ULxL.

3.2.2.3 QSPI NOR flash

A QSPI NOR flash is also available. It can e.g., serve as boot device or recovery device.
The following block diagram shows how the QSPI NOR flash is connected to the CPU.

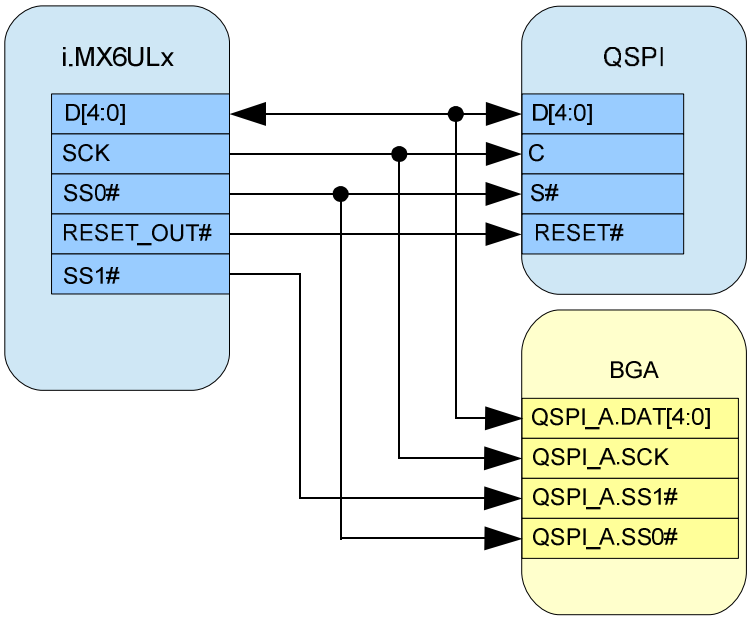

Illustration 6: Block diagram QSPI NOR flash interface

The QSPI NOR flash Reset-Out pin as well as the QSPI signals are routed to the TQMa6ULxL balls. See also 3.1.1.

The following table shows the QSPI NOR flash devices, which can be assembled on the TQMa6ULxL.

Table 15: QSPI NOR flash

Manufacturer	Part number	Size		Temperature range
Micron	MT25QL512ABB8E12-0SIT	512 Mbit	64 Mbyte	–40 °C to +85 °C
Micron	MT25QL02GCBB8E12-0SIT	2048 Mbit	256 Mbyte	–40 °C to +85 °C

Attention: QSPI NOR flash	
	QSPI_A.SS1# is primarily used for the eMMC. The BSP provided by TQ-Systems GmbH supports the Extended I/O protocol in STR mode.

3.2.2.4 EEPROM

A serial EEPROM for permanent storage of e.g. module characteristics or customers parameters is available as assembly option.
The I2C4 bus controls the EEPROM. Write-Protection (WP) is supported as an assembly option.
The following block diagram shows how the EEPROM is connected to the CPU.

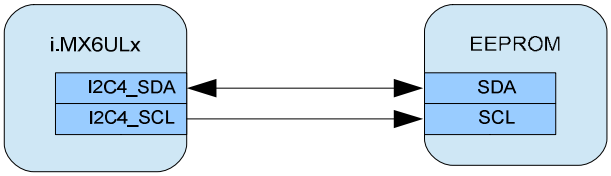

Illustration 7: Block diagram EEPROM interface

The following table shows details of the EEPROM.

Table 16: EEPROM

Manufacturer	Part number	Size	Temperature range
STM	24LC64T-I/MC	64 Kbit	–45 °C to +85 °C

- The EEPROM has I²C address `0x50 / 101 0000b`

3.2.2.5 Manufacturer EEPROM with temperature sensor

A serial EEPROM for permanent storage of e.g. module characteristics or customers parameters is available.
The I2C4 bus controls the EEPROM.
The lower 128 bytes (address 00h to 7Fh) can be set to Permanent Write Protected mode (PWP) or to Reversible Write Protected mode (RWP) by software. The upper 128 bytes (address 80h to FFh) cannot be write-protected and are available for general data storage. The device also contains a temperature sensor.

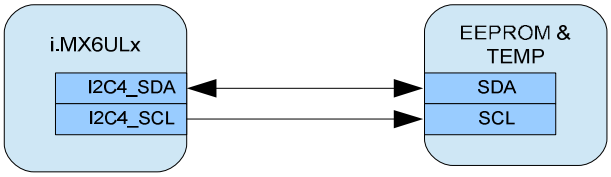

Illustration 8: Block diagram Manufacturer EEPROM with temperature sensor

The following table shows details of the Manufacturer EEPROM.

Table 17: Manufacturer EEPROM

Manufacturer	Part number	Size	Temperature range
NXP	SE97BTP	2 × 128 bytes	–45 °C to +85 °C

- The device provides the following I²C addresses:
  - EEPROM (normal): `0x52 / 101 0010b`
  - EEPROM (Protection mode): `0x32 / 011 0010b`
  - Temperature sensor: `0x1A / 001 1010b`

3.2.3 CPU-internal RTC

The i.MX6ULx provides an RTC, which has its own power domain (SNVS). The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The type FC-135 used on the TQMa6ULxL has a standard frequency tolerance of ±20 ppm @ +25 °C. (Parabolic coefficient: max. –0.04 ppm / °C²).
The following block diagram shows the implementation on the TQMa6ULxL.

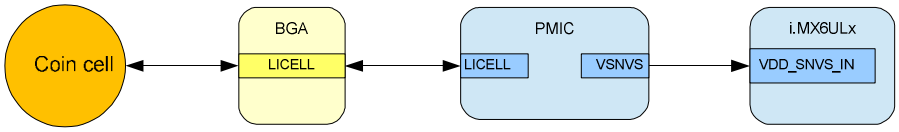

Illustration 9: Block diagram CPU-internal RTC

The RTC power domain SNVS of the CPU is supplied by the PMIC-internal regulator VSNVS. This regulator is supplied either by VIN or by LICELL. LICELL supports simple coin cells as well as Lithium coin cells or SuperCaps, which can also be charged by the PMIC. Charging methods and electrical characteristics of the LICELL pin are to be taken from the PMIC Data Sheet (7).

Note: RTC power consumption	
	A coin cell is not suitable for long term bridging on account of the high current consumption. A Lithium coin cell or a SuperCap might be an option depending on the use case. It is to be taken note of that the typical charging current is only 60 µA. For long term bridging an external RTC connected at the I²C bus is recommended.

3.2.4 External RTC

The i.MX6ULx provides an additional external RTC, which is controlled by I2C4. The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The type CM7V-T1A used on the TQMa6ULxL has a standard frequency tolerance of ±20 ppm @ +25 °C. (Parabolic coefficient: max. –0.035 ppm / °C²).
The following block diagram shows the implementation on the TQMa6ULxL.

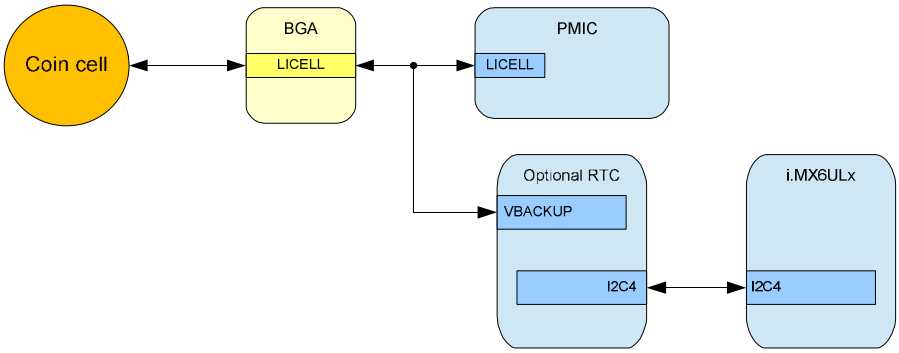

Illustration 10: Block diagram external RTC

The RTC power domain is supplied by VCC3V3_IN. LICELL is available as VBACKUP at the BGA pads. LICELL supports simple coin cells as well as Lithium coin cells or SuperCaps, which can also be charged by the PMIC. Charging methods and electrical characteristics of the LICELL pin are to be taken from the PMIC Data Sheet (7).

- The optional RTC has I²C address `0x68 / 110 1000b`

Note: RTC power consumption	
	A coin cell is not suitable for long term bridging because of the high current consumption. A Lithium coin cell or a SuperCap might be an option depending on the use case. It is to be taken note of that the typical charging current is only 60 µA. For long term bridging the external RTC connected at the I²C bus is recommended.

3.2.5 Interfaces

3.2.5.1 Overview

The TQMa6ULxL provides interfaces with primary functions. They can all be used simultaneously independent of their configuration. Some primary functions are not available if a secondary function is used.

Table 18: Internal interfaces

Interface	Qty.	Function	Section	Remark
USDHC	1	Primary	3.2.5.13	USDHC2 | eMMC, 8 data bits [15]
MMDC	1	Primary	3.2.2.1	DDR3L SDRAM, 16 data bits
QSPI	1	Primary	3.2.5.8	QSPI NOR flash, 4 data bits [15]

Table 19: External interfaces

Interface	Qty.	Function	Section	Remark
CCM	2	Secondary	–	Multiplexing has to be adapted
CSI	1	Secondary	–	Multiplexing has to be adapted
ECSPI	1	Primary	3.2.5.2	ECSPI2
ECSPI	2	Secondary	3.2.5.2	ECPSI1 / ECSPI3 / ECSPI4 | Multiplexing has to be adapted
EIM	1	Secondary	–	Multiplexing has to be adapted
ENET	2	Primary	3.2.5.3	RMII (10/100 Mbit/s) / 1588 | Multiplexing has to be adapted
EPIT	2	Secondary	–	Multiplexing has to be adapted
FLEXCAN	2	Primary	3.2.5.4	FLEXCAN[2:1]
GPIO	11	Primary	3.2.5.5	GPIO1 / GPIO4
GPT	2	Secondary	–	GPT[2:1] | Multiplexing has to be adapted
I^2C	2	Primary	3.2.5.6	I2C2 / I2C4
I^2C	2	Secondary	3.2.5.6	I2C1 / I2C3 | Multiplexing has to be adapted
KPP	1	Secondary	–	Multiplexing has to be adapted
LCDIF	1	Primary	3.2.5.7	Graphics interface
MQS	1	Secondary	–	Multiplexing has to be adapted
NAND	1	Secondary	–	Multiplexing has to be adapted
PWM	8	Secondary	–	PWM[8:1] | Multiplexing has to be adapted
SAI	3	Secondary	–	SAI[3:1] | Multiplexing has to be adapted
SIM	2	Secondary	–	Multiplexing has to be adapted
SJC	1	Primary	3.2.5.9	JTAG
SNVS	1	Primary	3.2.5.10	SNVS_TAMPER[9-0]
SRC	1	Secondary	–	Depends on BOOT_MODE0 | BOOT_MODE1
SPDIF	1	Secondary	–	Multiplexing has to be adapted
UART	3	Primary	3.2.5.11	UART1 / UART3 / UART6
UART	5	Secondary	3.2.5.11	UART2 / UART4 / UART[8:7] | Multiplexing has to be adapted
USB	2	Primary	3.2.5.12	USB_OTG1 / USB_OTG2
USDHC	1	Primary	3.2.5.13	SD card interface
WDOG	1	Primary	3.2.6	WDOG1#
WDOG	1	Secondary	3.2.6	WDOG[3:2] | Multiplexing has to be adapted
XTALOSC	1	Primary	3.2.5.14	CCM_CLK1_N / CCM_CLK1_P

In the following sections, only the external primary interfaces are described.

15: Corresponding BGA pads can be configured for external interfaces, if internal interfaces are not used.

3.2.5.2 ECSPI

The i.MX6ULx provides four full-duplex ECSPI interfaces, which can also be configured as Master/Slave. Primarily ECSPI2 is available at the TQMa6ULxL balls. The following table shows the signals used by the ECSPI2 interface.

Table 20: Signals ECSPI2

Signal name	Direction	TQMa6ULxL ball	Remark
ECSPI2_MISO	I	D11	–
ECSPI2_MOSI	O	C11	–
ECSPI2_SCLK	O	A11	–
ECSPI2_SS0	O	B11	–

3.2.5.3 Ethernet

The i.MX6ULx provides a 10/100 MAC core, which supports MII (4 bit) and RMII (2 bit). The RMII signals are available as primary function at the TQMa6ULxL balls. The following table shows the signals used by the RMII interface.

Table 21: Signals RMII

Signal name	Power-Group	Direction	TQMa6ULxL ball	Remark
ENET_MDC	NVCC_GPIO (3.3 V)	O	D6	–
ENET_MDIO		I/O	D5	–
ENET1_RDATA[1:0]	NVCC_ENET (2.5 V / 3.3 V)	I	B6:A6	–
ENET1_RX_EN		I	A5	–
ENET1_RX_ER		I	C5	–
ENET1_TDATA[1:0]		O	B8:A8	–
ENET1_TX_CLK		O	A7	–
ENET1_TX_EN		O	C7	–
ENET2_RDATA[1:0]		I	B2:A2	–
ENET2_RX_EN		I	B1	–
ENET2_RX_ER		I	C1	–
ENET2_TDATA[1:0]		O	B4:A4	–
ENET2_TX_CLK		O	A3	–
ENET2_TX_EN		O	C3	–

Note: NVCC_ENET

NVCC_ENET has to be connected externally!

The RMII interface of the i.MX6ULx can operate with an I/O voltage of 2.5 V or 3.3 V. In order to use the interface, additional signals of the ENET signal group are required. The accompanying power supply pin is routed to TQMa6ULxL ball F13 to operate these signals on the same I/O voltage, if RMII is used.
It is possible to use the MII interface with an adapted pin multiplexing. Details are to be taken from the Reference Manual and the CPU Data Sheet (1), (6).

Note: VCC3V3_REF_OUT

VCC3V3_REF_OUT has to supply an RMII PHY on the MBa6ULx with approximately 60 mA.
It has to be ensured that the load on the customer's carrier board is not higher than approximately 60 mA.

3.2.5.4 CAN

The i.MX6ULx provides two integrated CAN 2.0B controllers. Both signals pairs are available at the TQMa6ULxL balls.
The signal drivers required have to be implemented on the carrier board.
The following table shows the signals used by the CAN interface.

Table 22: Signals FLEXCAN

Signal name	Direction	TQMa6ULxL ball	Remark
FLEXCAN1_RX	I	R16	–
FLEXCAN1_TX	O	R17	–
FLEXCAN2_RX	I	T12	–
FLEXCAN2_TX	O	U12	–

3.2.5.5 GPIO

Beside their interface function, most i.MX6ULx pins can also be configured as GPIO.
All these GPIOs can trigger an interrupt. Details are to be taken from the Reference Manual and the CPU Data Sheet (1), (6).
In addition, several pins are already available as GPIO at the TQMa6ULxL balls.
The following table shows the GPIO signals provided.

Table 23: Signals GPIO

Signal name	Power-Group	Direction	TQMa6ULxL ball	Remark
GPIO1_IO09	–	I/O	N17	–
GPIO1_IO18	–	I/O	M17	–
GPIO1_IO19	–	I/O	M16	–
GPIO4_IO21	NVCC_CSI (1.8 V / 3.3 V)	I/O	T7	–
GPIO4_IO22		I/O	R7	–
GPIO4_IO23		I/O	U6	–
GPIO4_IO24[16]		I/O	R6	–
GPIO4_IO25		I/O	P6	–
GPIO4_IO26		I/O	U5	–
GPIO4_IO27		I/O	T5	–
GPIO4_IO28		I/O	R5	–

Note: NVCC_CSI	
	NVCC_CSI has to be connected externally!

The electrical characteristics of the GPIOs are to be taken from the CPU Data Sheet (1).

16: Can be used as temperature and PMIC interrupt. Further information can be found in the schematics.

3.2.5.6 I²C

The i.MX6ULx provides four I²C interfaces.
I2C2 and I2C4 are available as primary function and routed to the TQMa6ULxL balls.
The following table shows the signals used by the I²C interfaces.

Table 24: Signals I²C

Signal name	Power-Group	Direction	TQMa6ULxL ball	Remark
I2C2_SCL	NVCC_CSI (1.8 V / 3.3 V)	O	U8	–
I2C2_SDA		I/O	U7	–
I2C4_SCL	PU 2.2 kΩ to 3.3 V on TQMa6ULxL	O	U11	–
I2C4_SDA		I/O	T11	–

Note: NVCC_CSI	
	NVCC_CSI has to be connected externally!

The following table shows the I²C devices connected to the I2C4 bus on the TQMa6ULxL.

Table 25: Address assignment I2C4 bus

Component	Address
EEPROM (M24C64)	0x50 / 101 0000b
PMIC (MC32PF3000A7EP)	0x08 / 000 1000b
RTC (DS1339U-33) (optional)	0x68 / 110 1000b
Manufacturer EEPROM (SE97BTP) (Normal Mode)	0x52 / 101 0010b
Manufacturer EEPROM (SE97BTP) (Protection Mode)	0x32 / 011 0010b
Temperature sensor in Manufacturer EEPROM (SE97BTP)	0x1A / 001 1010b

If more devices are connected to the I2C4 bus on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional Pull-Ups should be provided at the I²C bus on the carrier board, if required.

3.2.5.7 eLCDIF

The i.MX6ULx CPU provides a display controller, which supports displays of different size and performance.
Information regarding types of displays and supported formats are to be taken from the CPU Reference Manual (6).
The LCD signals routed to the TQMa6ULxL balls as primary function.
The following table shows the signals used by the LCD interface.

Table 26: Signals LCD

Signal name	Direction	TQMa6ULxL ball	Remark
LCDIF_CLK	O	T1	–
LCDIF_DATA23	I/O	J4	–
LCDIF_DATA22	I/O	J3	–
LCDIF_DATA21	I/O	J2	–
LCDIF_DATA20	I/O	J1	–
LCDIF_DATA19	I/O	K4	–
LCDIF_DATA18	I/O	K3	–
LCDIF_DATA17	I/O	K1	–
LCDIF_DATA16	I/O	L4	–
LCDIF_DATA15	I/O	L3	–
LCDIF_DATA14	I/O	L2	–
LCDIF_DATA13	I/O	L1	–
LCDIF_DATA12	I/O	M4	–
LCDIF_DATA11	I/O	M3	–
LCDIF_DATA10	I/O	M1	–
LCDIF_DATA09	I/O	N4	–
LCDIF_DATA08	I/O	N3	–
LCDIF_DATA07	I/O	N2	–
LCDIF_DATA06	I/O	N1	–
LCDIF_DATA05	I/O	P4	–
LCDIF_DATA04	I/O	P3	–
LCDIF_DATA03	I/O	P1	–
LCDIF_DATA02	I/O	R3	–
LCDIF_DATA01	I/O	R2	–
LCDIF_DATA00	I/O	R1	–
LCDIF_ENABLE	O	U2	–
LCDIF_HSYNC	O	U3	–
LCDIF_RESET	O	T4	–
LCDIF_VSYNC	O	U4	–

Attention: Faulty boot procedure or malfunction	
	Measures have to be taken on the carrier board, to prevent errors caused by connected displays while reading the boot pins. It also has to be ensured that the pull-up or pull-down configuration resistors at the boot pins to not interfere with the display operation.

3.2.5.8 QSPI

The i.MX6ULx provides a Quad SPI interface, which is routed to the TQMa6ULxL balls.
A NOR flash on the carrier board can only be connected to the QSPI interface, when no eMMC is assembled on the TQMa6ULxL.
The following table shows the signals used by the Quad SPI interface.

Table 27: Signals QSPI

Signal name	Direction	TQMa6ULxL ball	Remark
QSPI_A_DATA3	I/O	G1	–
QSPI_A_DATA2	I/O	H1	–
QSPI_A_DATA1	I/O	G2	–
QSPI_A_DATA0	I/O	H2	–
QSPI_A_SS1#	O	G4	Only available on TQMa6ULxL without eMMC
QSPI_A_SS0#	O	G3	Only available on TQMa6ULxL without eMMC
QSPI_A_SCK	O	H4	–

Attention: Malfunction	
	The QSPI signal pins of the TQMa6ULxL have to be treated as NC, if not used on the carrier board. A NOR flash on the carrier board can only be connected to the QSPI interface, when no eMMC is assembled on the TQMa6ULxL. The QSPI interface may only be used as memory interface. The eCSPI interface may be used to connect other SPI devices.

3.2.5.9 SJC

The i.MX6ULx can operate in two different JTAG modes. The mode is defined by pin JTAG_MOD.
The following table shows the modes as well as the mode set on the TQMa6ULxL.

Table 28: JTAG modes

JTAG_MOD	Name	Remark
0	Daisy Chain All	For common SW debug (High speed and series production) ⇨ default
1	SJC only	IEEE® 1149.1 JTAG compliant mode

The following table shows the signals used by the JTAG interface.

Table 29: Signals JTAG

Signal name	Direction	TQMa6ULxL ball	Remark
JTAG_TCK	I	J7	i.MX6ULx-internal PU 47 kΩ
JTAG_TMS	I	G11	i.MX6ULx-internal PU 47 kΩ
JTAG_TDI	I	G10	i.MX6ULx-internal PU 47 kΩ
JTAG_TDO	O	G9	i.MX6ULx-internal keeper
JTAG_TRST#	I	J11	i.MX6ULx-internal PU 47 kΩ
JTAG_MOD	I	G7	PD 4.7 kΩ on TQMa6ULxL + i.MX6ULx-internal PU 100 kΩ

3.2.5.10 TAMPER

The i.MX6ULx provides protection against unauthorised opening or manipulation of a device by tamper detection. The TAMPER pins are available at the TQMa6ULxL balls. The following table shows the available signals.

Table 30: Signals TAMPER

Signal name	Direction	TQMa6ULxL ball	Remark
SNVS_TAMPER9	I	P11	–
SNVS_TAMPER8	I	R12	–
SNVS_TAMPER7	I	P12	–
SNVS_TAMPER6	I	R13	–
SNVS_TAMPER5	I	P13	–
SNVS_TAMPER4	I	N15	–
SNVS_TAMPER3	I	N14	–
SNVS_TAMPER2	I	K14	–
SNVS_TAMPER1	I	J14	–
SNVS_TAMPER0	I	H14	–

Details about the TAMPER pins function are to be taken from the CPU Reference Manual (6).

3.2.5.11 UART

The i.MX6ULx provides eight UART interfaces. No handshake signals are configured as primary function. More UARTs as well as handshake signals can be configured in the multiplexing. Details are to be taken from the CPU Reference Manual (6).

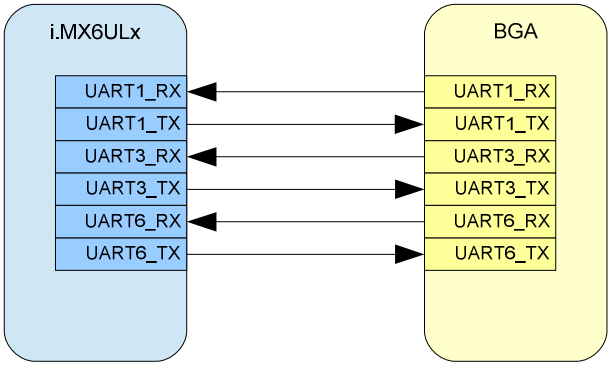

Illustration 11: Block diagram UART interfaces

The following table shows the signals used by the UART interfaces.

Table 31: Signals UART

Signal name	Direction	TQMa6ULxL ball	Remark
UART1_RX_DATA	I	L16	–
UART1_TX_DATA	O	L17	–
UART3_RX_DATA	I	P16	–
UART3_TX_DATA	O	P17	–
UART6_RX_DATA	I	P8	–
UART6_TX_DATA	O	R8	–

Note: UART1	
	UART1 is configured as RS-232 on the MBa6ULx.

3.2.5.12 USB

The i.MX6ULx provides two independent USB-OTG controllers with integrated High-Speed PHY. Both controllers can operate in Host or in Device mode. The signals of both controllers are available at the TQMa6ULxL balls as primary function.

The following table shows the signals used by the USB_OTG interfaces:

Table 32: Signals USB_OTG

Signal name	Direction	TQMa6ULxL ball	Remark
USB_OTG1_ID	I	F14	Device Mode: USB_OTG_ID signal is high Host Mode: USB_OTG_ID signal is low
USB_OTG1_OC	I	G15	–
USB_OTG1_PWR	O	F15	–
USB_OTG1_VBUS	P	F16	–
USB_OTG1_DN	I/O	E17	–
USB_OTG1_DP	I/O	G17	–
USB_OTG1_CHD#	O	D16	–
USB_OTG2_ID[17]	I	H15	Device Mode: USB_OTG_ID signal is high Host Mode: USB_OTG_ID signal is low
USB_OTG2_OC	I	J15	–
USB_OTG2_PWR	O	H16	–
USB_OTG2_VBUS	P	K16	–
USB_OTG2_DN	I/O	J17	–
USB_OTG2_DP	I/O	K17	

Note: USB mode	
	Currently the BSP provided by TQ-Systems GmbH only supports the Host mode.

17: If USB_OTG2_ID is not used the signal can be used to switch the NVCC_SD1 level.

3.2.5.13 USDHC

The i.MX6ULx provides a USDHC controller, which is the interface between Host system and SD/SDIO/MMC cards.
The USDHC1 port of the i.MX6ULx is routed to the TQMa6ULxL balls, to connect an MMC, SD, or SDIO card.

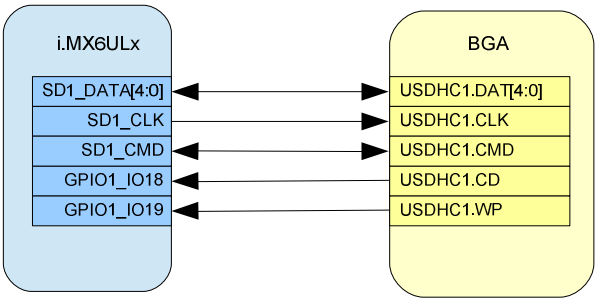

Illustration 12: Block diagram USDHC interface

The following table shows the signals used by the USDHC interface.

Table 33: Signals USDHC1

Signal name	Direction	TQMa6ULxL ball	Remark
USDHC1_CLK	O	U10	–
USDHC1_CMD	I/O	R10	–
USDHC1_DATA3	I/O	R9	–
USDHC1_DATA2	I/O	T9	–
USDHC1_DATA1	I/O	U9	–
USDHC1_DATA0	I/O	P10	–
USDHC1_CD#	I	M17	–
USDHC1_WP	O	M16	–

3.2.5.14 XTAL

The i.MX6ULx provides a programmable differential clock output, which is routed to the TQMa6ULxL balls.
CCM_CLK1_N/P can be configured as differential (LVDS) clock input or clock output.

The following table shows details of the XTAL signals.

Table 34: Signals XTAL

Signal name	Direction	TQMa6ULxL ball	Remark
CCM_CLK1_N	O	C17	–
CCM_CLK1_P	O	B17	–

3.2.6 Reset signals

Reset inputs or outputs are available at the TQMa6ULxL balls.
The following block diagram shows the wiring of the reset signals.

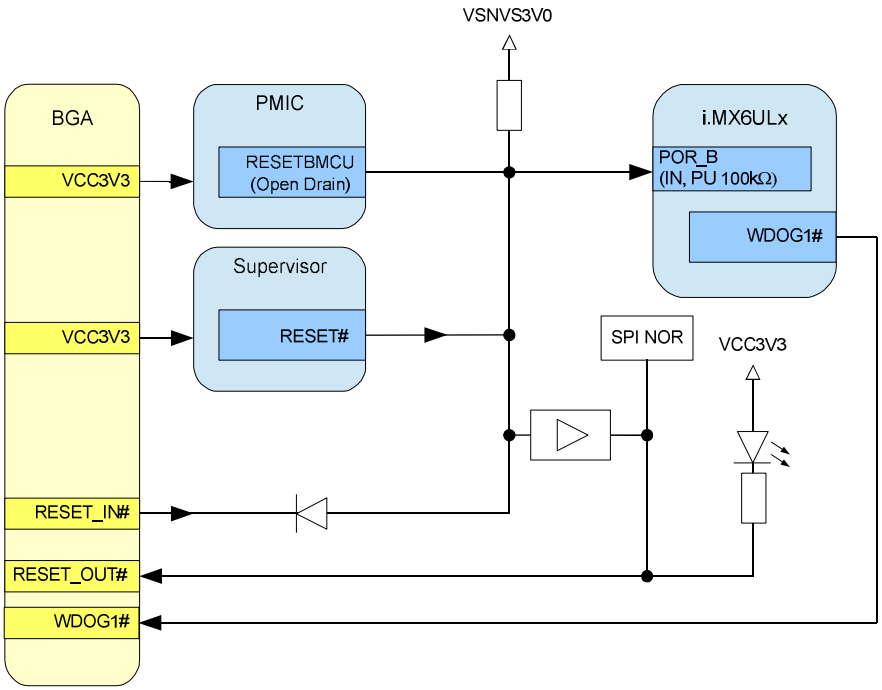

Illustration 13: Block diagram Reset

The following table describes the reset signals available at the TQMa6ULxL balls:

Table 35: Signals Reset

Signal name	Direction	TQMa6ULxL ball	Remark
RESET_IN#	$I_{PU\ 100k\Omega}$	T14	• Reset input POR_B (Power-On Reset) of the i.MX6ULx • Triggers COLD-Reset of the CPU • Low-active signal • Minimal duration to trigger a reliable Reset: app. 30 µs, see (6)
RESET_OUT#	O	U15	• Reset output RESETBMCU of the PMIC • Can be used to reset external periphery
WDOG1#	O	C9	• Low-active signal • Triggers Reset of the CPU in error case

Other RESET# sources are:

- VIN – RESET#
- PMIC – RESETBMCU

A red LED on the TQMa6ULxL indicates the RESET# condition.

3.2.7 Power supply

3.2.7.1 TQMa6ULxL power supply

The following block diagram shows the TQMa6ULxL power supply.

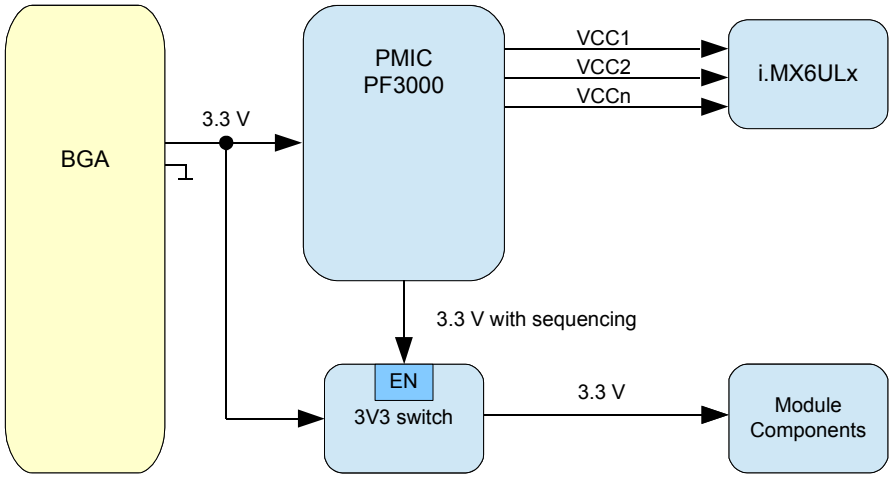

Illustration 14: Block diagram TQMa6ULxL power supply

The characteristics and functions of the single pins and signals are to be taken from the PMIC Data Sheet (7) and the CPU Reference Manual (6).

3.2.7.2 TQMa6ULxL power consumption

The given power consumption has to be seen as an approximate value. The TQMa6ULxL power consumption strongly depends on the application, the mode of operation and the operating system.

The following table shows TQMa6ULxL power supply and power consumption parameters:

Table 36: TQMa6ULxL power consumption

Mode of operation	Current @ 3.3 V_{IN}	Power @ 3.3 V_{IN}	Remark
U-Boot prompt	mA	mW	–
Linux prompt	mA	mW	–
Linux stress test	mA	mW	–
Suspend to RAM	mA	mW	–
Standby	mA	mW	–
Off-Mode	TBD	TBD	PMIC_PWRON = low
Reset	TBD	TBD	RESET_IN# = low

3.2.7.3 TQMa6ULxL supply voltages

In addition to the TQMa6ULxL supply voltage some internal voltages are provided at the TQMa6ULxL balls.
The following table shows the voltages provided.

Table 37: TQMa6ULxL supply voltages

Voltage	TQMa6ULxL ball	Remark
NVCC_CSI	N5	–
NVCC_ENET	E13	–
VCC1V8_OUT	D9	–
VCC2V5_OUT	D14	–
VCC3V3_IN	A9, B9	Used on the TQMa6ULxL, switched on by VCC3V3_V33_OUT
VCC3V3_REF_OUT	C10	–
VCC3V3_V33_OUT	E14	–
VCCCORE_OUT	D10	–
VCCDDR_OUT	E15	–
VDDARM_CAP	L7	–
VDDSOC_CAP	L8, L11	–
VSNVS_REF_OUT	C15	–

3.2.7.4 Other supply voltages

In addition to the 3.3 V VIN, the TQMa6ULxL offers voltage inputs for the USB OTG controllers.

Table 38: TQMa6ULxL USB_OTG supply voltages

Signal name	Direction	TQMa6ULxL ball	Remark
USB_OTG1_VBUS	P	F16	VBUS voltage for USB controller For details see i.MX6ULx data sheet (1)
USB_OTG2_VBUS	P	K16	

3.2.7.5 Voltage monitoring

The TQMa6ULxL features a supervisor which monitors the input voltage VIN.
If the input voltage is too low, a Reset is triggered until the input voltage is in the permitted range again.
The block diagram in Illustration 13 shows the wiring.
The Supervisor triggers typically at 2.93 V (min: 2.87 V / max: 2.99 V) and has a delay of 200 ms.
All other voltages generated on the TQMa6ULxL are routed to the TQMa6ULxL balls and can be monitored on the carrier board.

Attention: Destruction or malfunction	
	The voltage monitoring does not detect an exceedance of the permitted input voltage. An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa6ULxL.

3.2.7.6 Power-Up sequence TQMa6ULxL / carrier board

The TQMa6ULxL meets the required sequencing of the CPU (6) by using the PMIC (7).
The TQMa6ULxL operates with 3.3 V; the 3.3 V I/O voltage of the CPU signals is generated on the TQMa6ULxL.
This leads to requirements for the carrier board design concerning the chronological characteristics of the voltages generated on the carrier board.

Attention: Power-Up sequence	
	No TQMa6ULxL I/O pins may be driven by external components during the boot-process to avoid cross-supply and errors in the power-up sequence. To ensure a correct power-up, the following sequence must be met on the carrier board: The supply voltage of 3.3 V for the TQMa6ULxL is present and the carrier board supply of 3.3 V is activated by the TQMa6ULxL pin VCC3V3_REF_OUT.

The following block diagram shows the voltage regulator control on the carrier board:

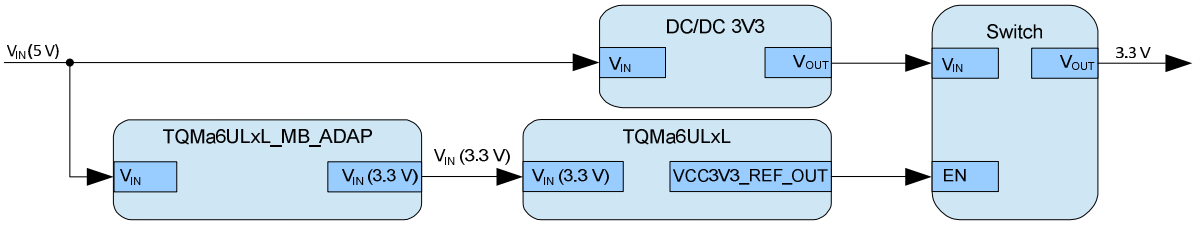

Illustration 15: Block diagram power supply carrier board

➢ The BOOT_MODE and BOOT_CFG pins have dedicated reference voltages, which are present at the right time.

3.2.7.7 Power modes

- Suspend to RAM (deep sleep mode – DSM)
- Standby

DSM und Standby are extremely efficient energy saving modes, in which parts of the core supply are switched off.
Details are to be taken from the CPU Reference Manual (6). These features have to be supported by the software.

3.2.7.8 PMIC

The characteristics and functions of all pins and signals have to be taken from the CPU Reference Manual (6) and the PMIC Data Sheet (7). The PMIC is connected to the I2C4 bus.

The following block diagram shows the connection between PMIC and CPU:

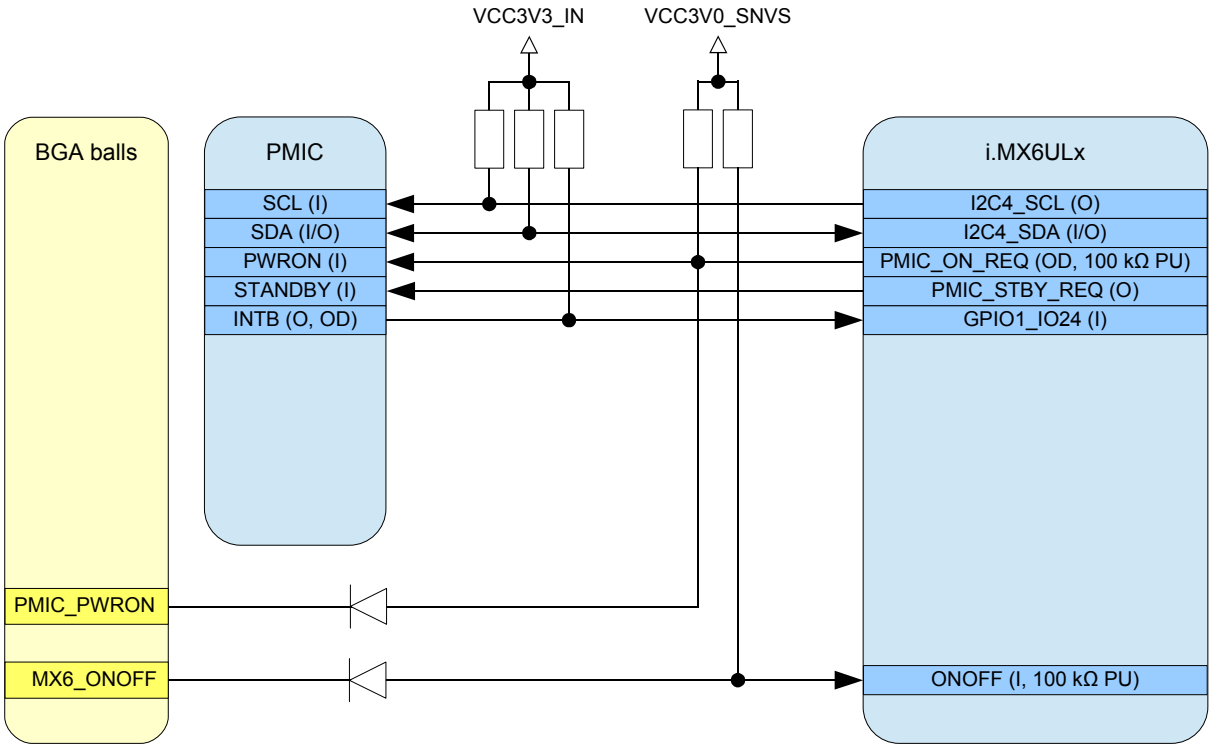

Illustration 16: Block diagram PMIC interface

- The PMIC has I²C address `0x08 / 000 1000b`

4. MECHANICS

4.1 TQMa6ULxL balls

The pins assignment listed in Table 2 refers to the corresponding BSP provided byTQ-Systems GmbH.
For information regarding I/O pins in Table 2, refer to the CPU pins.

4.2 Dimensions

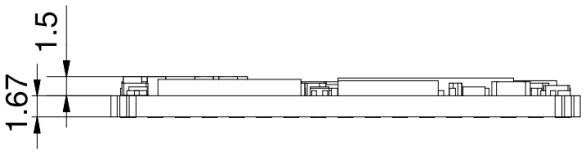

Illustration 17: Height of TQMa6ULxL

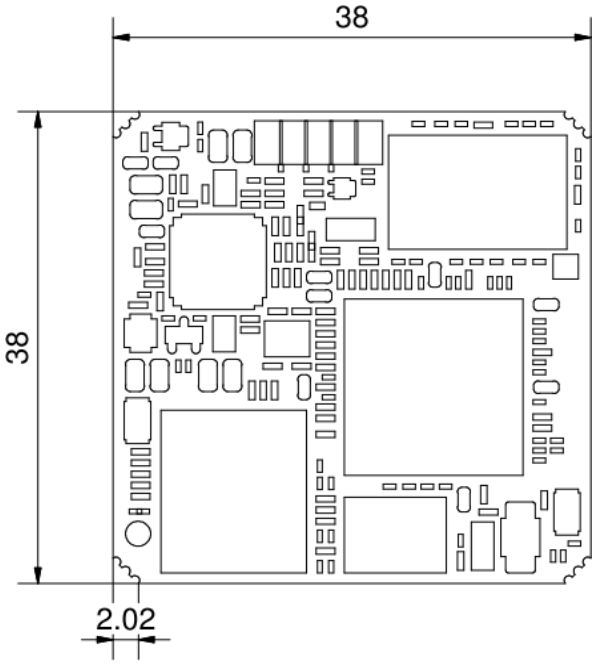

Illustration 18: Dimensions, top view TQMa6ULxL

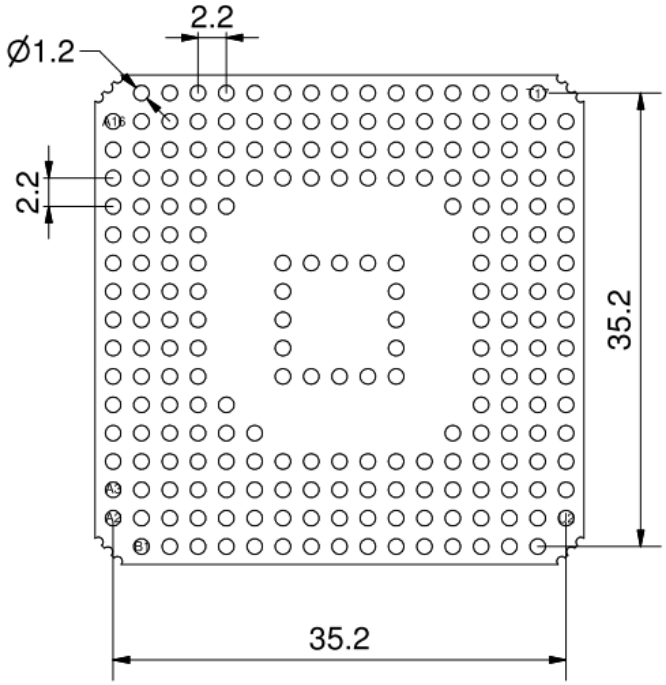

Illustration 19: Dimensions, **top view through TQMa6ULxL**

4.3 Component placement

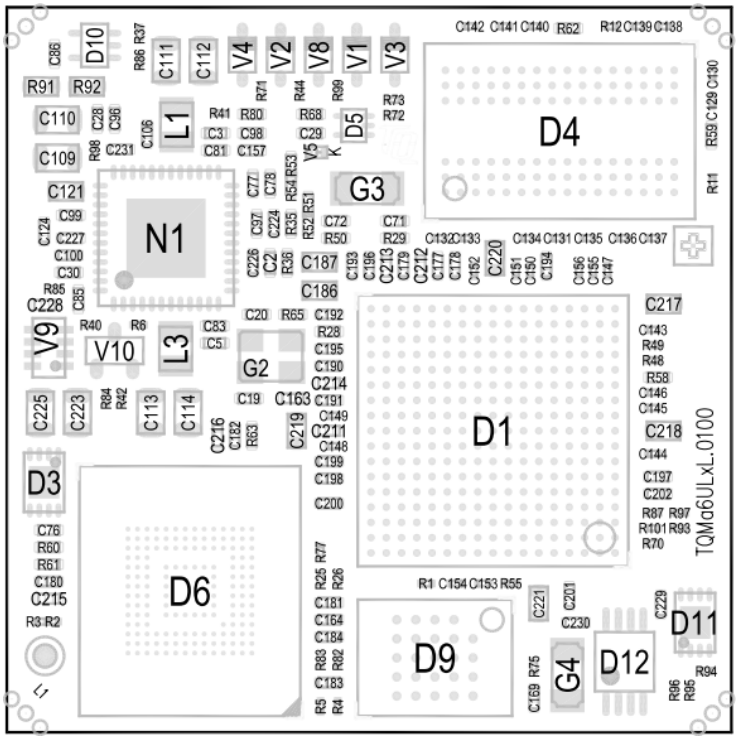

Illustration 20: Component placement

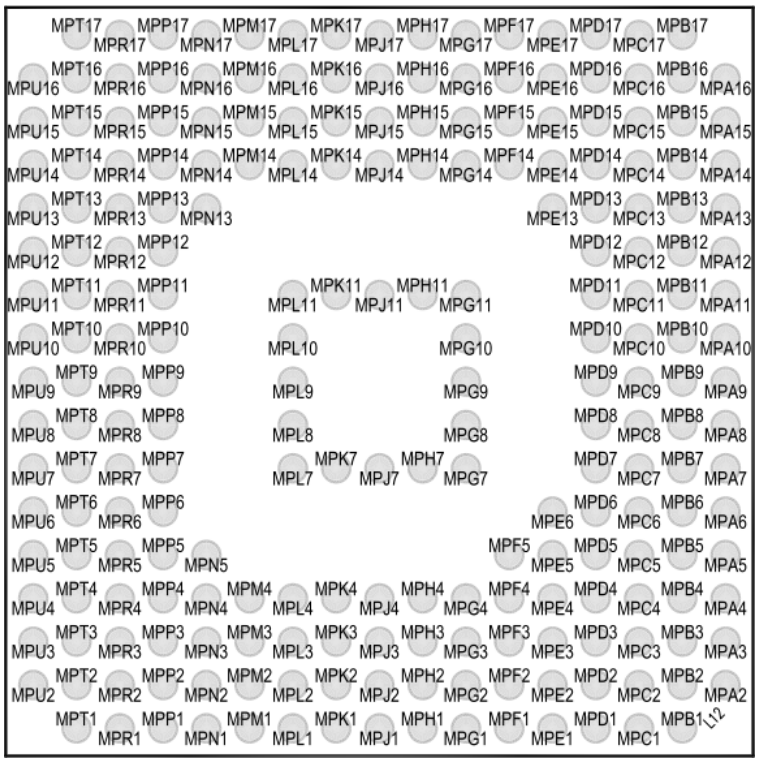

Illustration 21: Ball numbering scheme

4.4 Adaptation to the environment

The TQMa6ULxL has overall dimensions (length × width × height) of 38 × 38 mm × 3.3 mm³.
The TQMa6ULxL has a maximum height above the carrier board of approximately 3.3 mm.
The TQMa6ULxL weighs approximately 8 g ±1 g.

4.5 Protection against external effects

As an embedded module, the TQMa6ULxL is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMa6ULxL, a theoretical maximum of approximately 6.65 W have to be dissipated.
The power dissipation originates primarily in the CPU, the DDR3L SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See NXP documents (3) and (7) for further information.

Attention: Destruction or malfunction	
	The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the customers' responsibility to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Care of the tolerance chain (PCB thickness, PCB curvature, BGA balls, BGA housing, thermal gap pad, and heat sink) must be taken when connecting the TQMa6ULxL thermally to a housing. The CPU is not necessarily the highest component. Insufficient cooling may cause malfunction, destruction or accelerated ageing of the TQMa6ULxL.

4.7 Structural requirements

The TQMa6ULxL has to be soldered on the carrier board.

5. SOFTWARE

The TQMa6ULxL is delivered with a preinstalled boot loader U-Boot.
The BSP provided by TQ-Systems GmbH is configured for the TQMa6ULxL / MBa6ULx.
The boot loader U-Boot provides TQMa6ULxL-specific as well as board-specific settings, e.g.:

- CPU configuration
- PMIC configuration
- SDRAM configuration
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

More information can be found in the Support Wiki for the TQMa6ULx.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa6ULxL was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

Since the TQMa6ULxL operates on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.

The TQMa6ULxL it designed to pass the following test:

- EMC-Interference radiation:
  Measurement of electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 6 GHz according to DIN EN 55022 A1:2007.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa6ULxL.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signals: RC filtering, perhaps Zener diode(s)
- Fast signals: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤3.3 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 39: Climate and operational conditions extended temperature range –25 °C to +85 °C

Parameter	Temperature range	Remark
Chip temperature CPU i.MX6ULx	–40 °C to +105 °C	Typical max +90 °C
Environment temperature CPU i.MX6ULx	–40 °C to +85 °C	–
Chip temperature PMIC	–40 °C to +125 °C	–
Environment temperature PMIC	–40 °C to +85 °C	–
Package temperature DDR3L-SDRAM	–40 °C to +85 °C	–
Package temperature other ICs	–25 °C to +85 °C	–
Permitted storage temperature TQMa6ULxL	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Table 40: Climate and operational conditions industrial temperature range –40 °C to +85 °C

Parameter	Temperature range	Remark
Chip temperature CPU i.MX6ULx	–40 °C to +105 °C	Typical max +90 °C
Environment temperature CPU i.MX6ULx	–40 °C to +85 °C	–
Chip temperature PMIC	–40 °C to +125 °C	–
Environment temperature PMIC	–40 °C to +85 °C	–
Package temperature DDR3L-SDRAM	–40 °C to +85 °C	–
Package temperature other ICs	–40 °C to +85 °C	–
Permitted storage temperature TQMa6ULxL	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the CPUs' thermal characteristics is to be taken from NXP documents (3) and (7).

6.5 Reliability and service life

The theoretical MTBF for the TQMa6ULxL is approximately 1,472,325 hours with a constant error rate @ +40 °C Ground Benign.

The TQMa6ULxL is designed to be insensitive to shock and vibration.

Detailed information concerning the CPUs' service life under different operational conditions is to be taken from the NXP Application Note (4).

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa6ULxL is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

7.2 WEEE®

The company placing the product on the market is responsible for the observance of WEEE® regulation.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

7.3 REACH

The EU-chemical regulation 1907/2006 (REACH regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200.000. Thus the TQMa6ULxL always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa6ULxL on account of available Standby or Sleep-Modes of the components on the TQMa6ULxL.

7.5 Battery

No batteries are assembled on the TQMa6ULxL.

7.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa6ULxL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa6ULxL is delivered in reusable packaging.

7.7 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 41: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CCM	Clock Control Module
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
DC	Direct Current
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrie Norm (German industry standard)
DSM	Deep Sleep Mode
ECSPI	Enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIM	External Interface Module
eLCDIF	Enhanced LCD Interface
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	European Standard (Europäische Norm)
EPIT	Enhanced Periodic Interrupt Timer
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GPT	General Purpose Timer
HS	High-Speed
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Integrated Interchip Sound
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
IPU	Image Processing Unit
JTAG®	Joint Test Action Group
KPP	Key Pad Port
LCD	Liquid Crystal Display
LCDIF	LCD Interface
LDO	Low Drop-Out
LED	Light Emitting Diode
LICELL	Lithium Cell
LVDS	Low-Voltage Differential Signalling
MAC	Media Access Control
MDIO	Management Data Input/Output
MII	Media-Independent Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MMDC	Multi-Mode DDR Controller
MQS	Medium Quality Sound
MTBF	Mean operating Time Between Failures

Table 41: Acronyms (continued)

Acronym	Meaning
n/a	Not Applicable
NA	Not Available
NAND	Not-And
NC	Not Connected
NOR	Not-Or
OTG	On-The-Go
PC	Personal Computer
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
RWP	Reversible Write Protection
SAI	Serial Audio Interface
SD/eSD/SDXC	Secure Digital / enhanced Secure Digital / SD eXtended Capacity
SD/MMC	Secure Digital Multimedia Card
SDIO	Secure Digital Input/Output
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SJC	System JTAG Controller
SNVS	Secure Non-Volatile Storage
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SRC	System Reset Controller
SVHC	Substances of Very High Concern
SW	Software
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
USB-OTG	Universal Serial Bus On-The-Go
USDHC	Ultra-Secured Digital Host Controller
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 42: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 6UltraLite Applications Processors for Industrial Products IMX6ULxIEC_rev1.pdf	Rev. 1, 04/2016	NXP
(2)	Chip Errata for the i.MX 6UltraLite IMX6ULxCE_rev1.pdf	Rev. 1, 04/2016	NXP
(3)	i.MX 6UltraLite Power Consumption Measurement AN5170_power_rev2.pdf	Rev. 2, 05/2016	NXP
(4)	i.MX 6UltraLite Product Usage Lifetime Estimates AN5198_life_rev1.pdf	Rev. 1, 04/2016	NXP
(5)	Hardware Development Guide for the i.MX 6UltraLite Applications Processor IMX6ULxHDG_rev1.pdf	Rev. 1, 03/2016	NXP
(6)	i.MX 6UltraLite Applications Processor Reference Manual IMX6ULxRM_rev1.pdf	Rev. 1, 04/2016	NXP
(7)	Power management integrated circuit (PMIC) for i.MX7 & i.MX 6SL/SX/UL	Rev. 7, 03/2016	NXP
(8)	MBa6ULx User's Manual	– current –	TQ-Systems
(9)	Support-Wiki for the TQMa6ULx	– current –	TQ-Systems
(10)			

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