EH-MA46

Bluetooth® Technology Transmit Data Module

- **Bluetooth radio**
  - Fully embedded Bluetooth® v2.1+EDR
  - Class1 module
  - TX power +17dbm,-84dbm RX sensitivity
  - 128-bit encryption security
  - Range up to 300m
  - Integrated chip antenna or U.FL port
  - Multipoint capability(7devices connected at the same time)
- **Support profiles**
  - SPP (Master and slave)
  - iAP (ipod accessory protocol)
  - HID (Slave)
- **User interface**
  - Send AT command over UART
  - Firmware upgrade over USB
  - With SPP service active: 560kbps transmission speed (UART)
  - PCM interface
  - I2C interface(Master)
- **General I/O**
  - 10 general purpose I/Os
  - 2 analogue I/O
- **FCC and Bluetooth® qualified**
- **Single voltage supply: 3.3V typical**
- **Small form factor: 25.8 x 13.4 x 2.2mm**
- **Operating temperature range: -40 °C to 85 °C**

Version 2.1
July 21 2014

1. Contents

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1. Description

The EH-MA46 is an easy to use Bluetooth module, compliant with Bluetooth v2.1+EDR. The module provides complete RF platform in a small form factor.

The EH-MA46 enables electronic devices with wireless connectivity, not requiring any RF experience or expertise for integration into the final product. The EH-MA46 module, being a certified solution, optimizes the time to market of the final application.

The module is designed for maximum performance in a minimal space including fast speed UART and 10 general purpose I/O lines, 2 analogue I/O lines, several serial interface options, and up to 600 kbps transmission speed with SPP service active, 200 kbps with iAP service active.

The module is internal antenna and 26MHz crystal. Embedded Bluetooth AT command firmware is a friendly interface, Support different Bluetooth profiles, such as SPP, HID, iAP and etc. iAP over Bluetooth using apple's authentication coprocessor.

Customers using the Apple authentication IC must register as developers, to become an Apple certified MFI member. License fees may apply, for additional information visit: http://developer.apple.com/programs/which-program/index.html.

Certified MFI developers developing electronic accessories that connect to an iPod®, iPhone®, and iPad® can gain access to technical documentation, hardware components, technical support and certification logos.

Customized firmware for peripheral device interaction, power optimization, security, and other proprietary features may be supported and can be ordered pre-loaded and configured.

2. Application

- Serial cable replacement
- M2M industrial control
- Service diagnostics
- Data acquisition equipment
- Machine controls
- Sensor monitoring
- Security systems
- Mobile health.

3. EH-MA46 Product numbering

EH-MA46(B)

A. EH ---------- Company Name(Ehong)
B. MA46 ---------- Module Name , Antenna
C. B ---------- U.FL Connector

4. Electrical Characteristic

4.1. Recommend operation conditions

Operating Condition	Min	Typical	Max	Unit
Operating Temperature Range	-40	-	+85	°C
Supply Voltage	+2.7	+3.3	+3.7	V
AIO Voltage	-	-	1.8	V
PIO Voltage	+2.7	3.3	+3.7	V
RF frequency	2400	2441	24800	MHz

Table 1: Recommended Operating Conditions

4.2. Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature Range	-40	+120	°C
PIO Voltage	-0.4	+3.7	V
AIO Voltage	-0.4	1.8	V
VDD Voltage	-0.4	+3.7	V
Other Terminal Voltages except RF	-0.4	VDD+0.4	V

Table 2: Absolute Maximum Rating Recommended Operating Conditions

4.3. Power consumptions

Operating Condition	Min	Typical	Max	Unit
Standby, without deep sleep	1.23	1.77	-	mA
Standby, with deep sleep	0.05	0.28	-	mA
Inquiry window time [b]	-	-	40	mA
Connected (Deep sleep disable, sniff[a] enable)	1.23	3	10	mA
Connected (Deep sleep on, sniff[a] enable)	0.02	1.5	10	mA
Connected with data transfer	5	15	30	mA

Table 3: Power consumptions

Note :
Power consumption depends on the firmware used. Typical values are shown in the table.
[a]Sniff mode ----- In Sniff mode, the duty cycle of the slave's activity in the piconet may be reduced. If a slave is in active mode on an ACL logical transport, it shall listen in every ACL slot to the master traffic,

unless that link is being treated as a scatter net link or is absent due to hold mode. With sniff mode, the time slots when a slave is listening are reduced, so the master shall only transmit to a slave in specified time slots. The sniff anchor points are spaced regularly with an interval of Tsniff.
[b]Radio on(Inquiry)----Search time is 22 seconds

4.4. Input/output Terminal Characteristics

4.4.1. Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low	-0.4	-	+0.8	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.2	V
V_{OH} output logic level high, I_{OH} = -4.0mA	VDD-0.2	-	-	V
Input and Tri-state Current				
Strong pull-up	-100	-40	-10	μA
Strong pull-down	10	40	100	μA
Weak pull-up	-5	-1.0	-0.2	μA
Weak pull-down	0.2	+1.0	5.0	μA
I/O pad leakage current	-1	0	+1	μA
C_I Input Capacitance	1.0	-	5.0	pF

Table 4: Digital Terminal

4.4.2. USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
V_{IL} input logic level low	-	-	0.3VDD	V
V_{IH} input logic level high	0.7VDD	-	-	V
Input Leakage Current				
GND < VIN < VDD[a]	-1	1	5	μA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD	V

Table 5: USB Terminal

(a) Internal USB pull-up disable

5. Pinout and Terminal Description

5.1. Pin Configuration

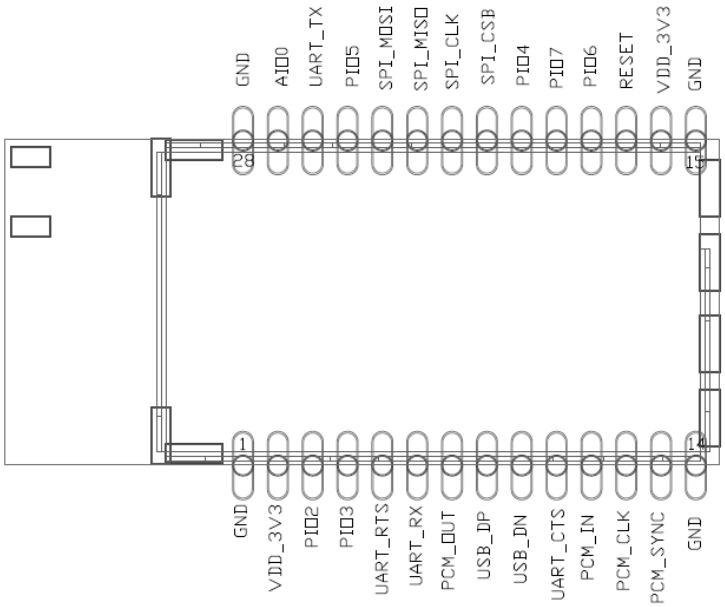

Figure 1: Pinout of EH-MA46

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	VDD_3V3	3V3 power input	3V3 power input
3	PIO2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
4	PIO3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
5	UART_RTS	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
6	UART_RX	CMOS input with weak internal pull-down	UART data input
7	PCM_OUT	CMOS output, tristate, with weak internal pull-down	Synchronous Data Output
8	USB_DP	Bi-directional	USB data plus with selectable internal 1.5K pull-up resistor
9	USB_DN	Bi-directional	USB data minus
10	UART_CTS	CMOS input with weak internal pull-down	UART clear to send active low
11	PCM_IN	CMOS Input, with weak internal pull-down	Synchronous Data Input

12	PCM_CLK	Bi-directional with weak internal pull-down	Synchronous Data Clock
13	PCM_SYNC	Bi-directional with weak internal pull-down	Synchronous Data Sync
14	GND	Ground	Ground
15	GND	Ground	Ground
16	VDD_3V3	3.3V power input	3.3V power input
17	RESET	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
18	PIO6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
19	PIO7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
20	PIO4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
21	SPI_CSB	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
22	SPI_CLK	input with weak internal pull-down	Serial Peripheral Interface clock
23	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
24	SPI_MOSI	CMOS input, with weak internal pull-down	Serial Peripheral Interface data input
25	PIO5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
26	UART_TX	CMOS output, tristate, with weak internal pull-up	UART data output
27	AIO0	Bi-directional	Programmable input/output line
28	GND	Ground	Ground

Table 6：PIN Terminal Description

6. Physical Interfaces

6.1. Power Supply

The module DC3.3V power input.
Power supply pin connection capacitor to chip and pin as far as possible close
Capacitor decouples power to the chip
Capacitor prevents noise coupling back to power plane.

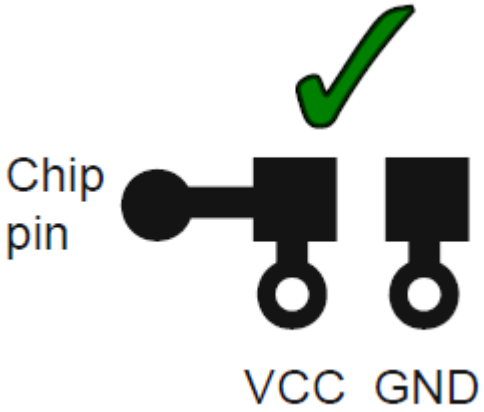

Figure 2: Power Supply PCB Design

6.2. Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via software configured watchdog timer.

The RESETB pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

Pin Name / Group	Pin Status on Reset
PIOs	Input with weak pull-down
AIOs	Output, driving low
PCM_OUT	Tristated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	PD
UART_TX	Output tristated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tristaed with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Tristated with weak pull-down
RESETB	Input with weak pull-up

Table 7: Pin Status on Reset

6.3. PIO

EH-MA46 has a total of 10 digital programmable I/O terminals. They are powered from VDD (3.3V). Their functions depend on firmware running on the device. PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs.

Note:

All PIO lines are configured as inputs with weak pull-downs at reset.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes.

6.4. AIO

EH-MA46 has 2 analogue I/O terminals. Their functions depend on software. Typically ADC functions can be configured to battery voltage measurement. They can also be used as a digital PIO.

6.5. UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

The UART CTS and RTS signals can be used to implement RS232 hardware flow control where both are active low indicators.

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	3M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

Table 8: Possible UART Settings

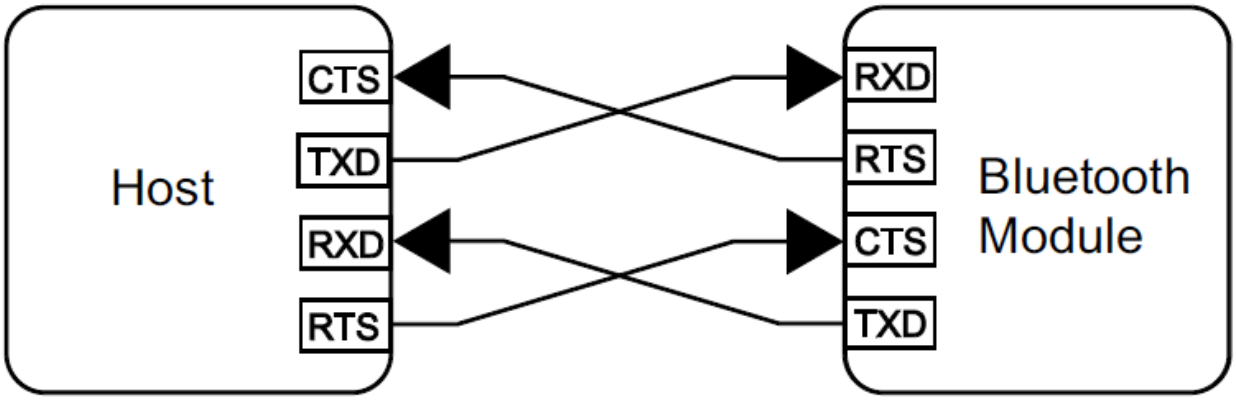

Figure 3： Connection To Host device

6.6. I2C Master

PIO6, PIO7 and PIO8 can be used to form a master I^2C interface. The interface is formed using software to drive these lines. It is suited only to relatively slow functions such as driving a LCD, keyboard scanner or EEPROM. In the case, PIO lines need to be pulled up through 2.2K**Ω** resistors.

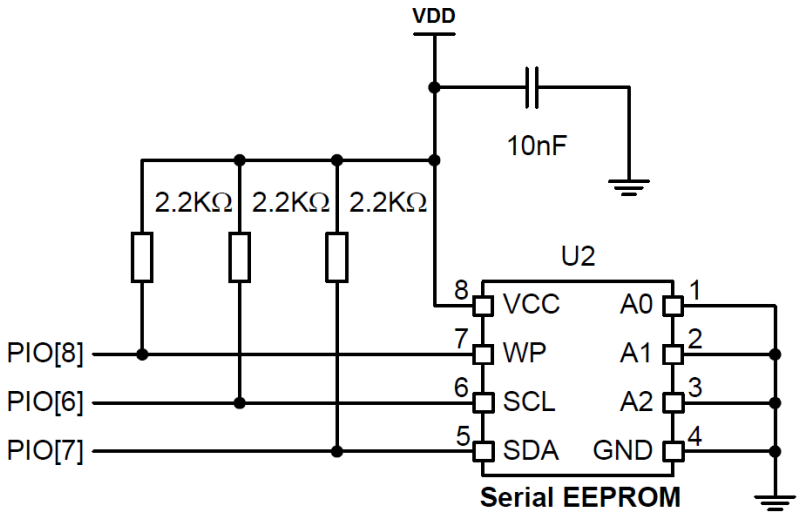

Figure 4 : Example EEPROM Connection with I2C Interface

6.6.1. Apple iOS CP reference design

The figures below give an indicative overview of what the hardware concept looks like. A specific MFI co-processor layout is available for licensed MFI developers from the MFI program.

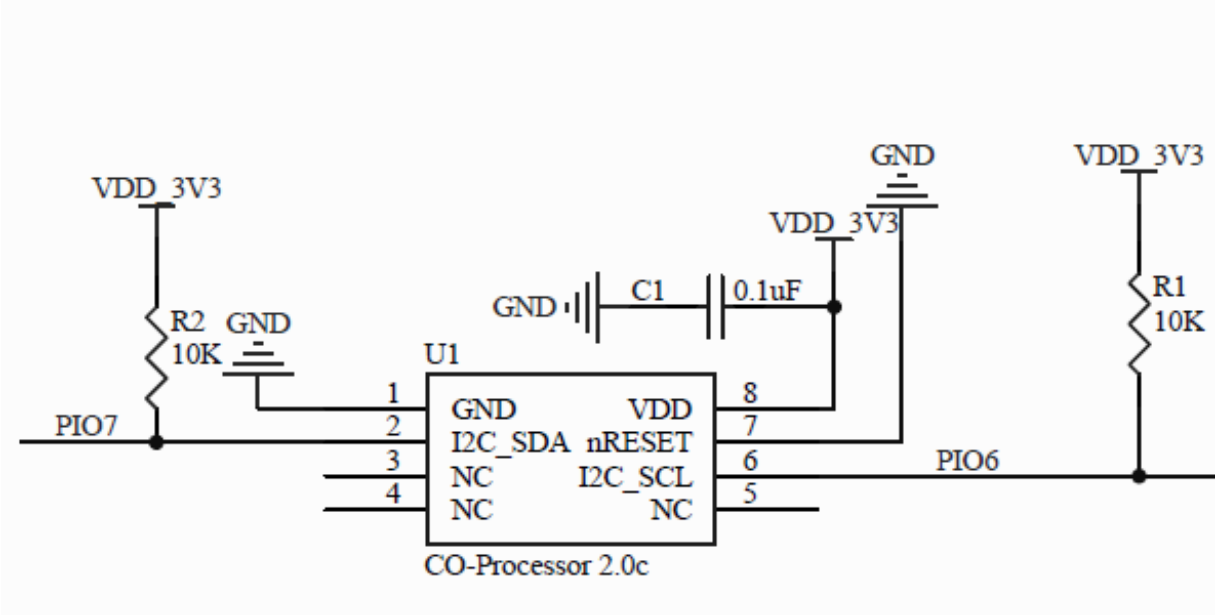

Figure 5 : Apple Co-processor 2.0C

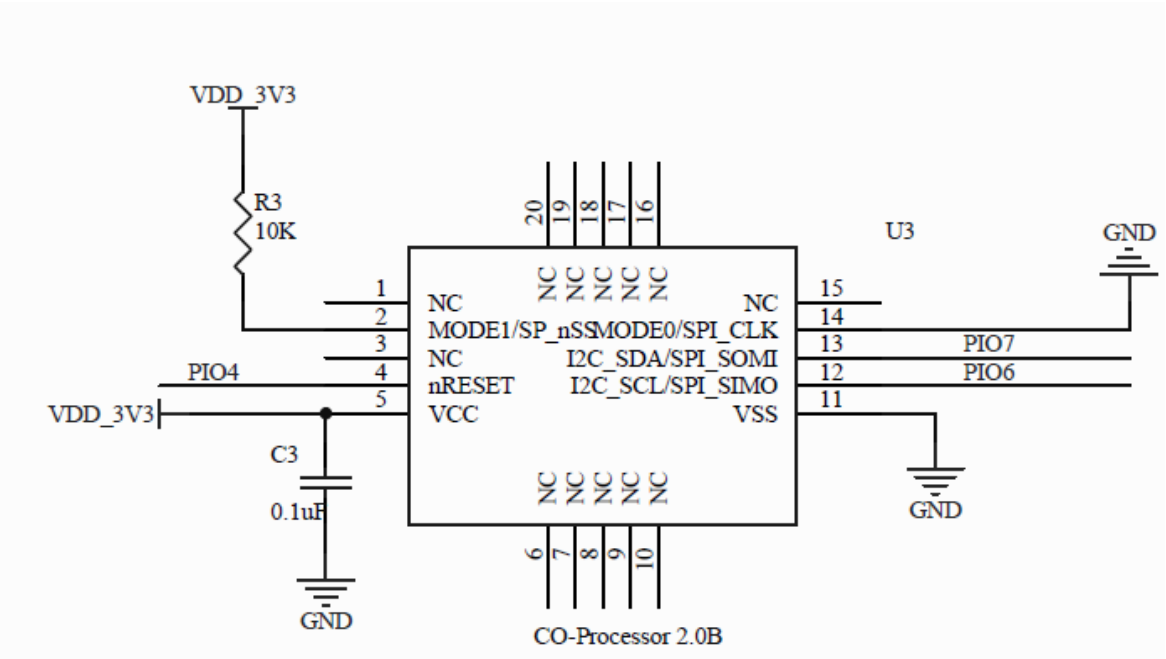

Figure 6 : Apple Co-processor 2.0B

6.7. PCM interface

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, the module has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for applications. The module offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on the module allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

The module can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. The module is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit µ-law or A-law companied sample formats at 8k samples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

The module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channels A-law and µ-law CODEC
- Motorola MC145481 8-bit A-law and µ-law CODEC

- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- The module is also compatible with the Motorola SSI™ interface.

6.7.1. PCM Interface Master/Slave

When PCM is configured as a master, the module generates PCM_CLK and PCM_SYNC.

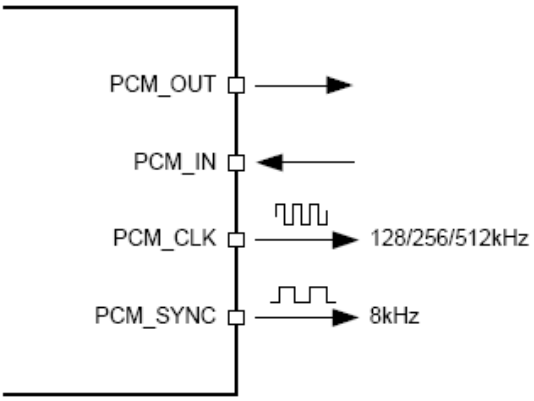

Figure 7: Configured PCM as a Master

When PCM is configured as the slave, the module accepts PCM_CLK rates up to 2048kHz.

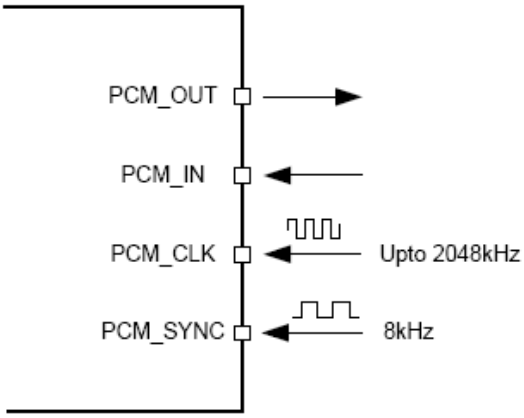

Figure 8: Configured PCM as a Slave

6.7.2. Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When the module is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When the module is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

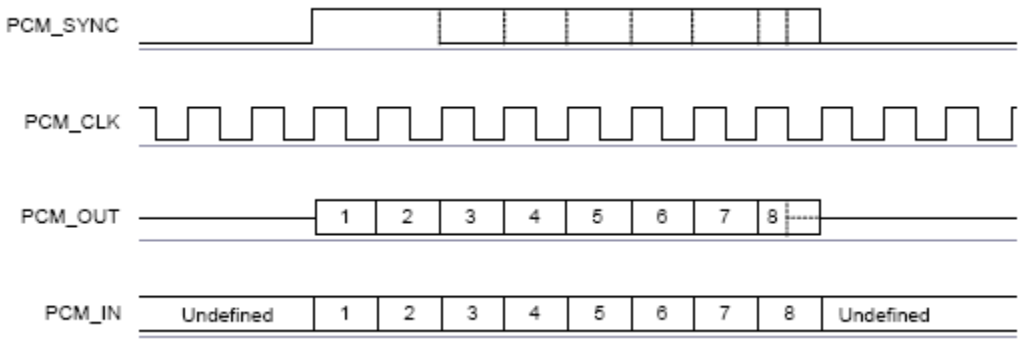

Figure 9: Long Frame Sync (Shown with 8-bit Companded Sample)

6.7.3. Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

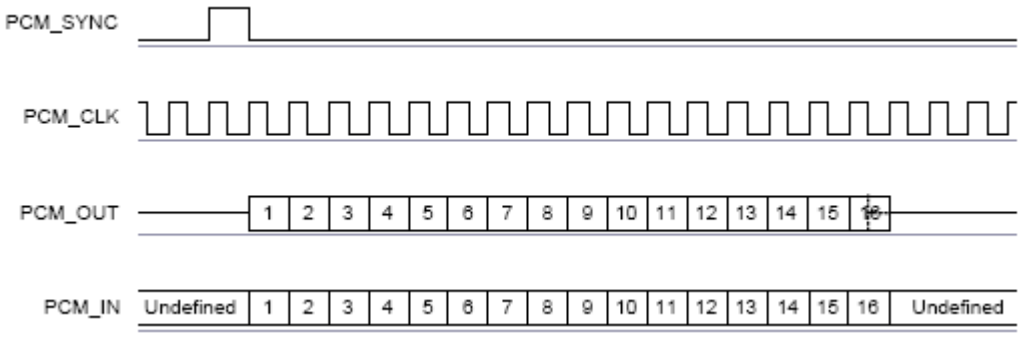

Figure 10: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, the module samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

6.7.4. Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

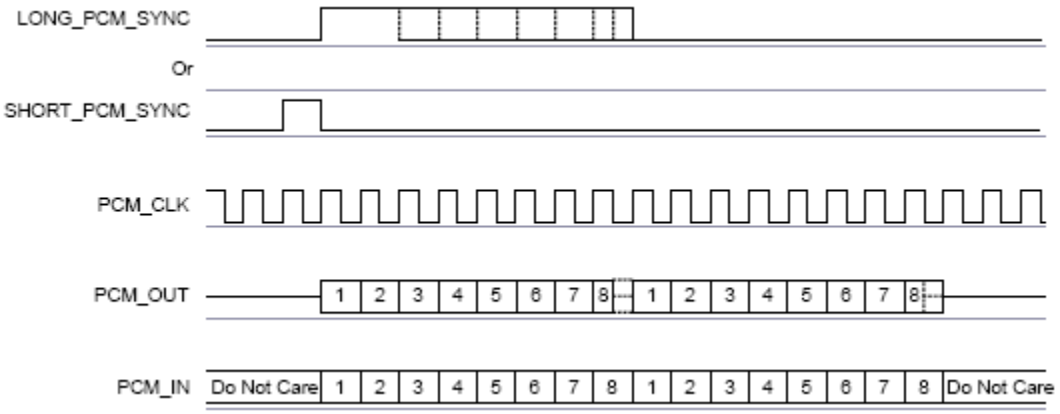

Figure 11: Multi-Slot Operation with Two Slots and 8-bit Companded Samples

6.7.5. GCI Interface

The module is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

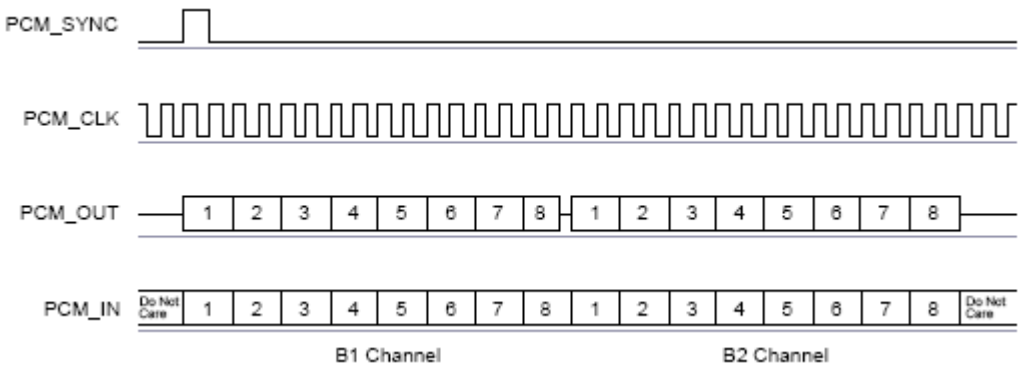

Figure 12: GCI Interface

The start of a frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With the module in slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

6.7.6. Slots and Sample Formats

The module can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats. The module supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8k samples/s. The bit order may be little or big endian. When 16-bit

slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

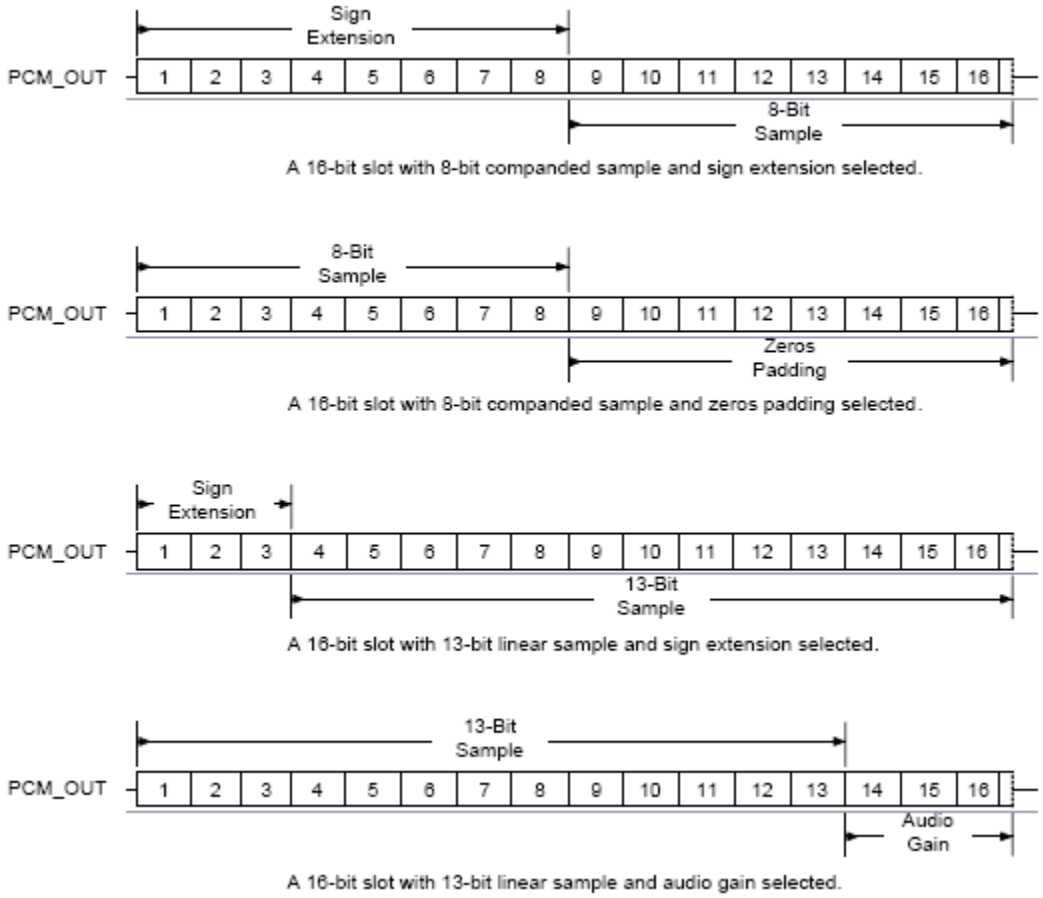

Figure 13: 16-Bit Slot Length and Sample Formats

6.7.7. Additional Features

The module has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

6.7.8. PCM Timing Information

Symbol	Parameter		Min	Typical	Max	Unit
f_{mclk}	PCL_CLK Frequency	4MHz DDS generation. Selection of frequency is	-	128 256	-	kHz

		programmable.		512		
		48MHz DDS generation. Selection of frequency is programmable.	2.9		-	kHz
	PCM_SYNC frequency		8	-		kHz
t_{mclkh}[(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl}[(a)]	PCM_CLK low	4MHz DDS generation	730	-		ns
	PCM_CLK jitter	48MHz DDS generation	-		21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 9: PCM Master Timing

[(a)] Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

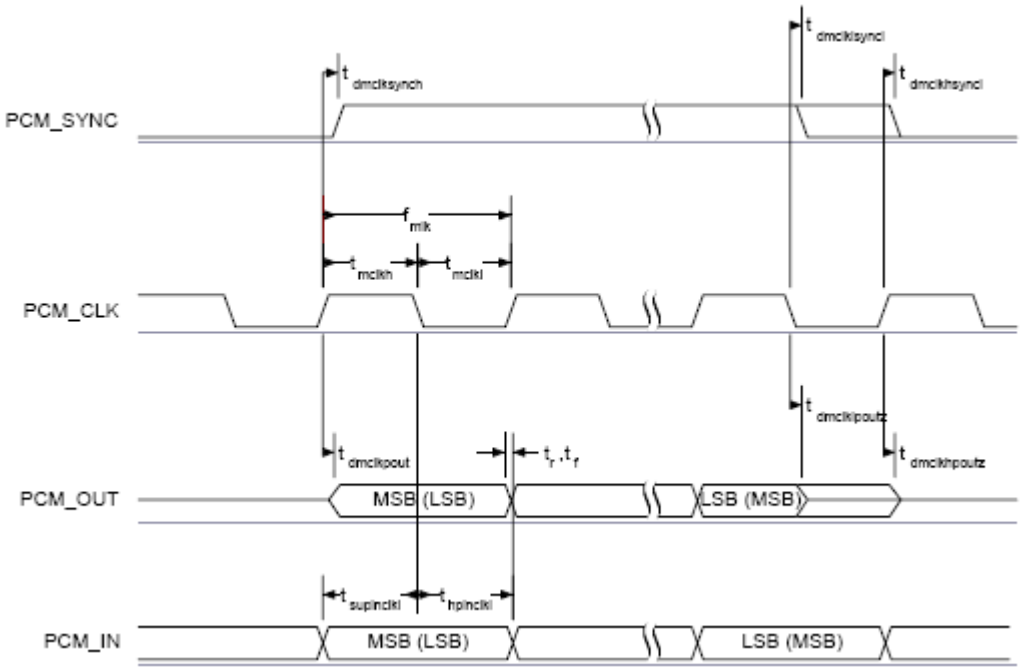

Figure 14: PCM Master Timing Long Frame Sync

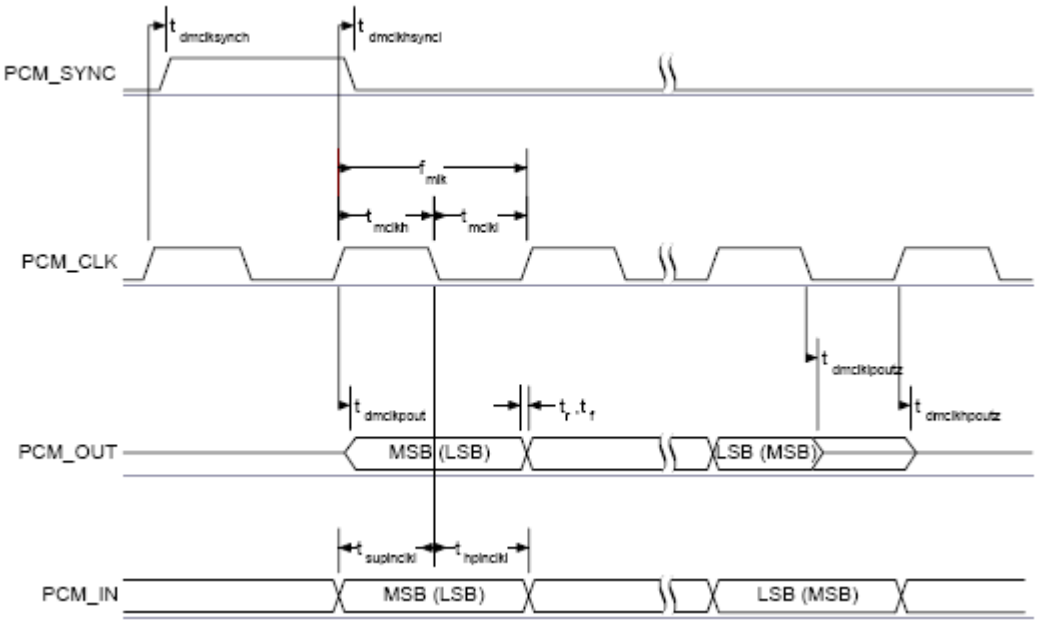

Figure 15: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typical	Max	Unit
fsclk	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
fsclk	PCM clock frequency (GCI mode)	128	-	4096	kHz
tsclkl	PCM_CLK low time	200	-	-	ns
tsclkh	PCM_CLK high time	200	-	-	ns
thsclksynch	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
tsusclksynch	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
tdpout	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
tdsclkhpout	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
tdpoutz	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
tsupinsclkl	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
thpinsclkl	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 10: PCM Slave Timing

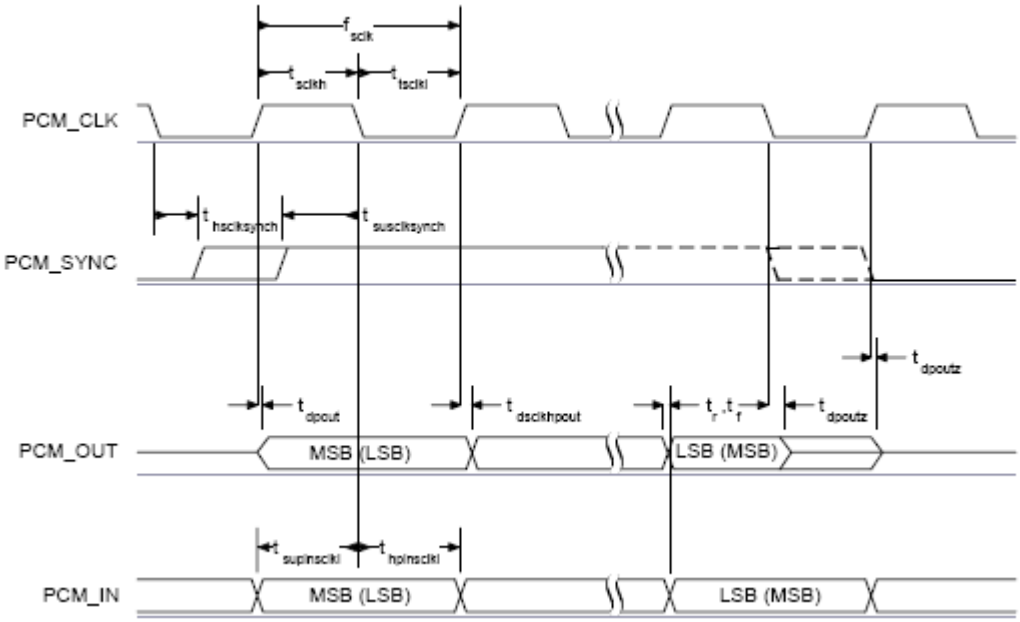

Figure 16: PCM Slave Timing Long Frame Sync

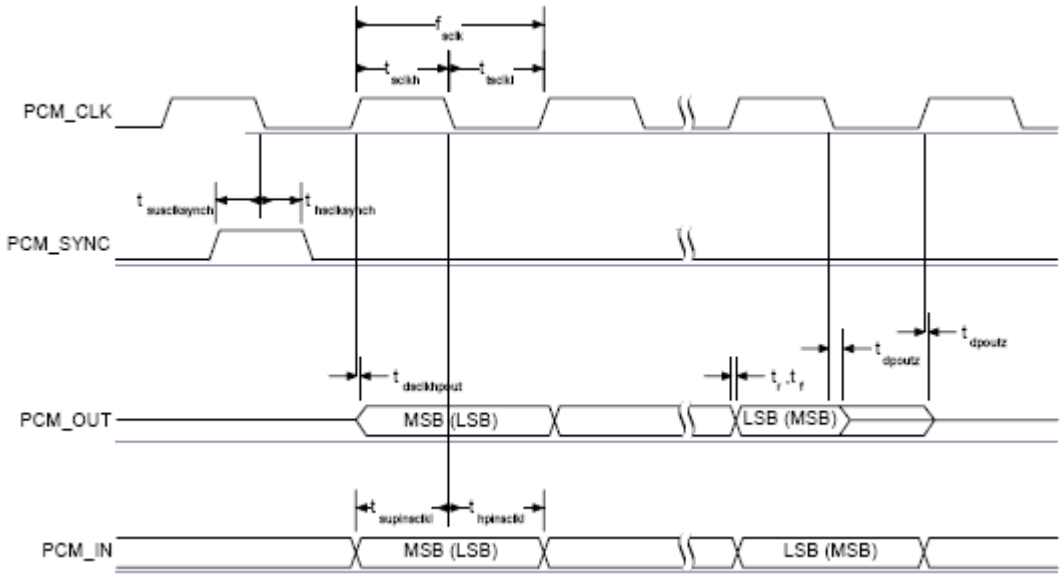

Figure 17: PCM Slave Timing Short Frame Sync

6.8. USB

This is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.1+EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

The module has an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device.

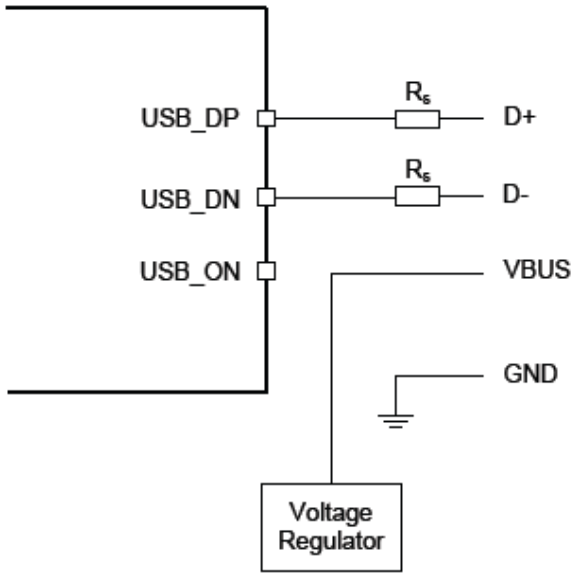

Figure 18: USB Connections

Identifier	Value	Function
R_s	27Ω Nominal	Impedance matching to USB cable

Table 11: USB Interface Component Values

Note:

USB_ON is only used when the firmware need an input to detect if USB is connected and the USB function shall be enabled. In such case it is shared with the module PIO terminals. If detection is not needed (firmware already runs with USB, such as USB DFU or USB CDC), USB_ON is not needed.

7. EH-MA46 Reference Design

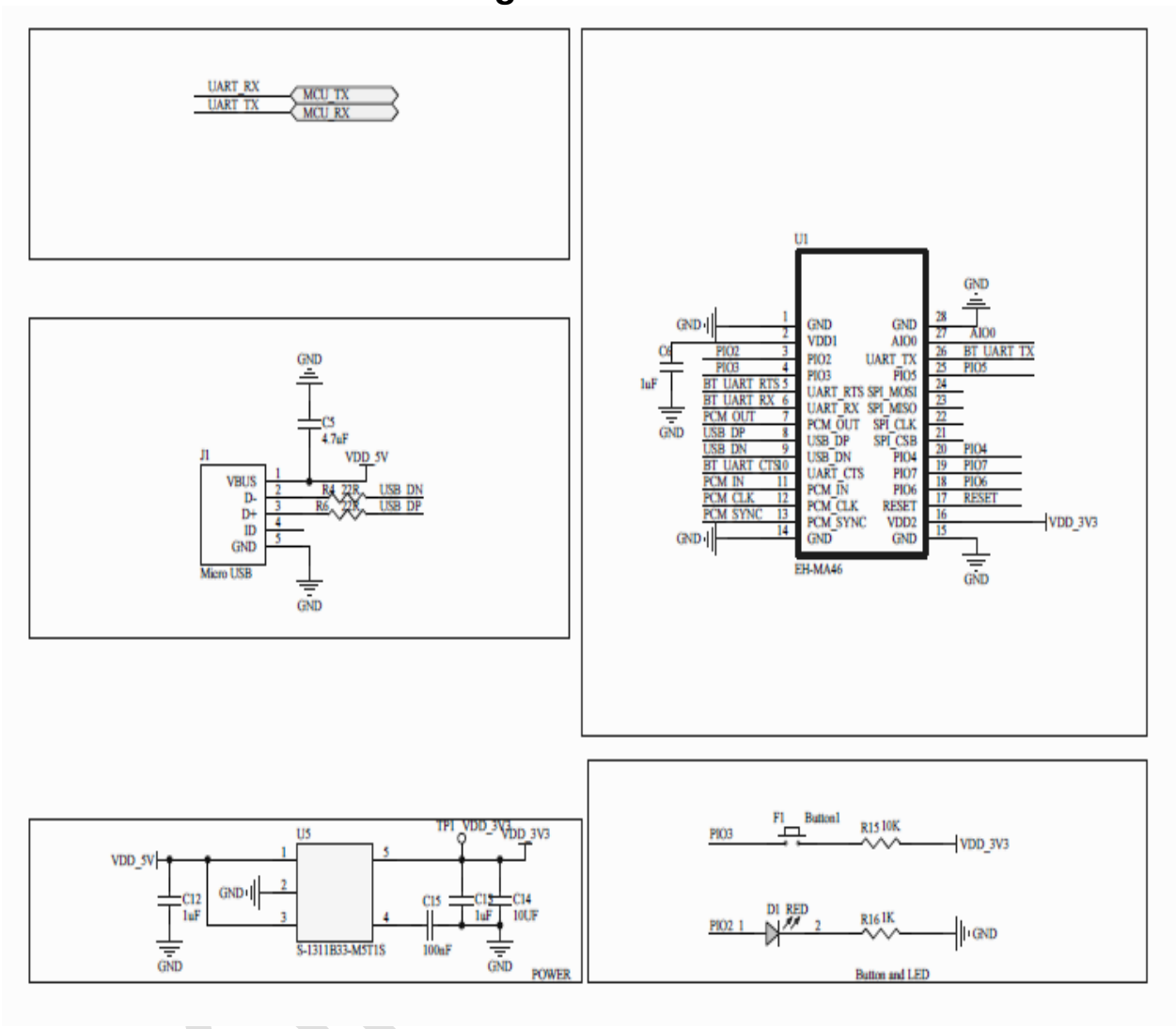

Figure 19: Reference Design

8. Mechanical and PCB Footprint Characteristics

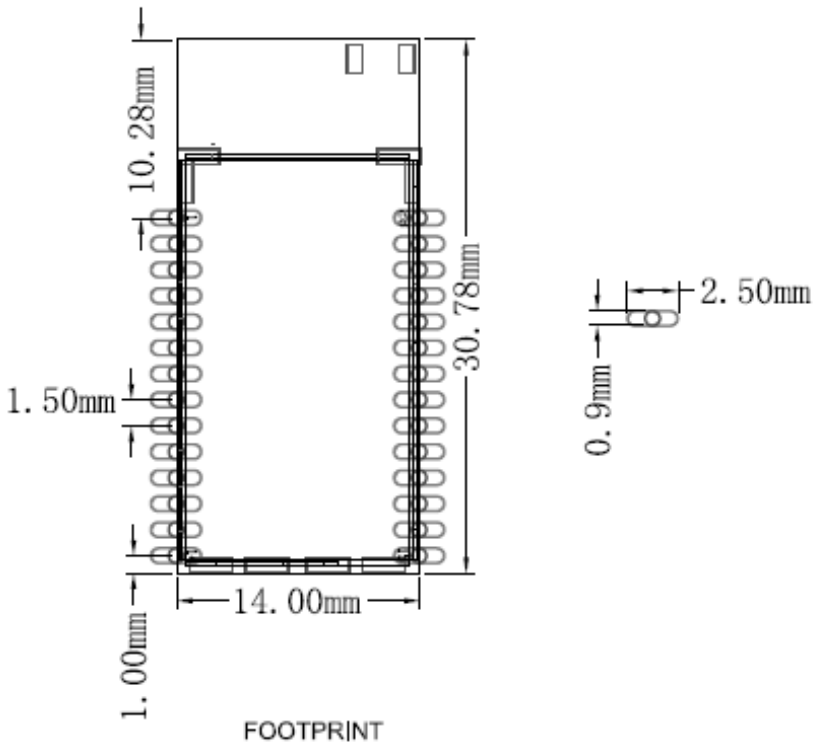

Figure 20: Recommended PCB Mounting Pattern (Unit: mm, Deviation:0.02mm)TOP View

9. RF Layout Guidelines

EH-MA46 has an on-board PCB antenna. PCB design to ensure enough clearance area of antenna, area length is 1.6 times of antenna length, area width is 4 times of antenna width, the bigger the better if the space allows. The specific size as shown figure below.

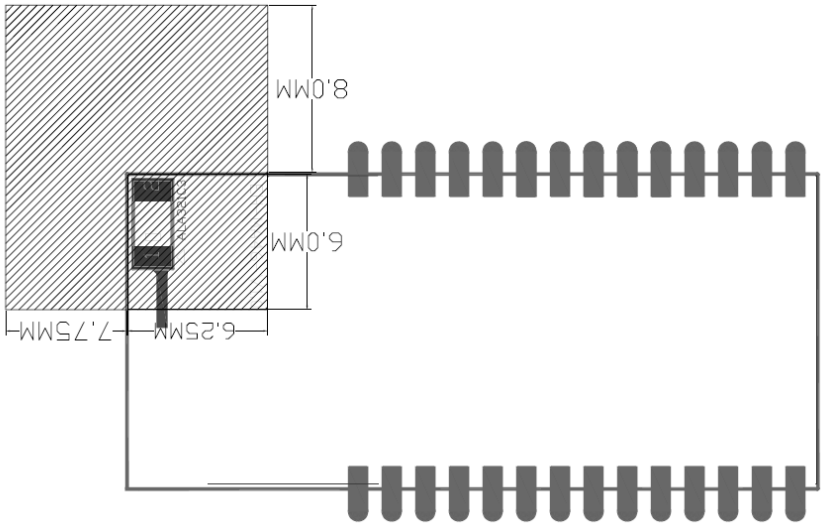

Figure 21: Clearance area of antenna

10. Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

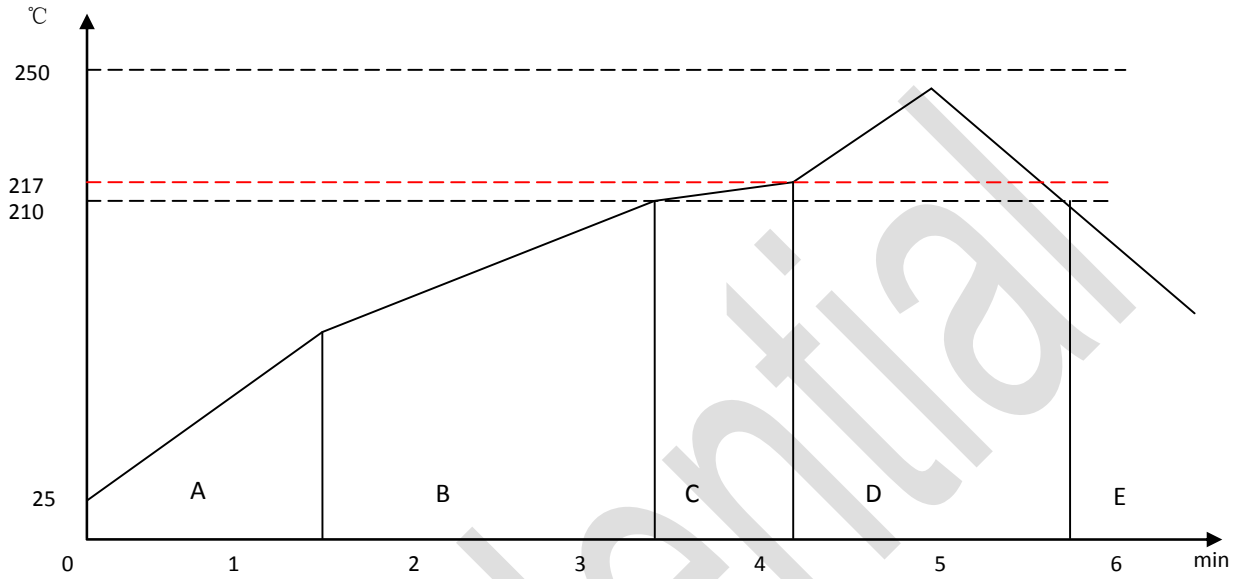

Figure 22: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone**.

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling ate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4 °C**.

11. Contact Information

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